A 0.18 µm differential LNA with reduced power consumption

A thesis submitted in partial fulfillment

Of the requirements for the degree of

Master of Technology

In

VLSI Design & Embedded Systems

By

Mala Narayana Swamy

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Rourkela-769 008, Odisha, India
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Under the guidance of

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NATIONAL INSTITUTE OF TECHNOLOGY
ROURKELA

CERTIFICATE

This is to certify that the work done for the direction of thesis entitled "**A 0.18 µm differential LNA with reduced power consumption**", submitted by **Mr. Mala Narayana Swamy (211EC2089)** in partial fulfillment of the requirements for the award of Master of Technology degree in Electronics and Communication Engineering with specialization in VLSI Design and Embedded Systems during session 2011-2013 at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any degree or diploma.

Date:
Place: NIT Rourkela

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M. Narayana Swamy

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Dedicated To

My Beloved Parents

ABSTRACT

The growth of wireless services and other telecom applications has increased the demand of low-cost Radio-Frequency Integrated Circuits (RFICs) and pushed the semiconductor industry towards complete system-on-chip solutions. This work presents the design of an inductively source degenerated CMOS differential cascode Low Noise Amplifier (LNA) and without source degenerated CMOS differential cascode Low Noise Amplifier (LNA) operating at 2 GHz frequency. LNA is an electronic device used to amplify weak signals before it can be fed to other parts of the receiver. A good LNA has a low noise figure (NF), a large enough gain and low power consumption. During reception of radio signal sent by satellite in a communication system, in the receiver section, second element after antenna is LNA. The receiver is the most power hungry block and the power consumption should be as low as possible. So, noise figure and power consumption are no less important issues than gain.

A Differential Cascode Low Noise Amplifier can be treated as a CS-CG two stage amplifier. An inductor is added at the drain of the main transistor to reduce the noise contribution of the cascode transistors. Another inductor connected at the gate of the cascode transistor and capacitive cross-coupling are strategically combined to reduce the noise and to increase power gain of the cascode transistors in a Differential Cascode LNA. It can reduce the power consumption, and increase the power gain of the LNA. The area occupied by the proposed design measured from the layout is observed as 1.111 mm × 1.27 mm. The LNA is designed with the 0.18 μm standard CMOS process. Cadence design tool Spectre_RF is used to design and simulation based on resistors, inductors, capacitors and transistors.

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CHAPTER 1

Introduction

1.1 Introduction of Low Noise Amplifier

The growth of wireless services and other telecom applications has pushed the semiconductor industry towards complete system-on-chip solutions. Wireless systems comprise of a front-end and a back-end section. The front-end section processes analog signals in the high radio frequency (RF) range while the back-end section processes analog and digital signals in the baseband low frequency range. Radio frequency (RF) refers to the frequency range in the electromagnetic spectrum that is used for radio communications [1]. It lies typically from 100 KHz to 100 GHz. However in general, frequencies below 1 GHz are considered baseband frequencies while those greater are described as RF.

The main goal of a designer is to obtain a design that meets the specifications in quick time. RF circuits must process analog signals with a wide dynamic range at high frequencies. RF components constitute a very small fraction of the whole chip. This is mainly because RF IC design involves a lot of tradeoffs in power, linearity, gain, frequency, and noise in the "RF design hexagon" shown in Figure1.1.1.

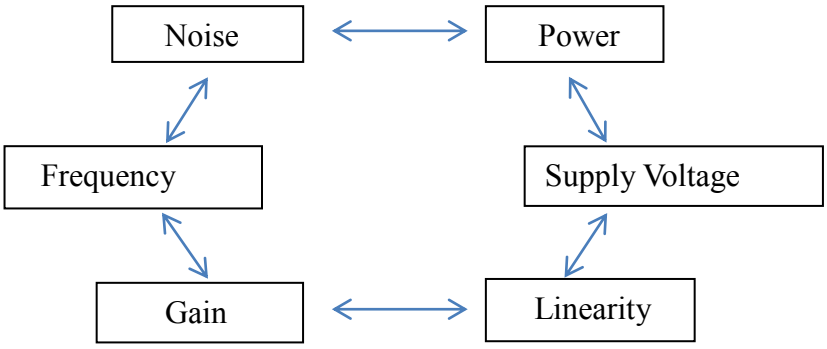


Fig. 1.1.1: RF design hexagon

RF design hexagon, where at least any two of six parameters trade with each other to some extent. Low noise amplifiers are the mainstay of radio frequency communication receivers and by knowing the specifications we can estimate the overall noise performance of the RF

Receivers. The radio frequency signal received at the antenna is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal before it can be fed to other parts of the receiver. Such an amplifier is referred to as a Low Noise Amplifier (LNA). LNA is the first active amplification block in the receiving path as shown in Figure 1.1.2.

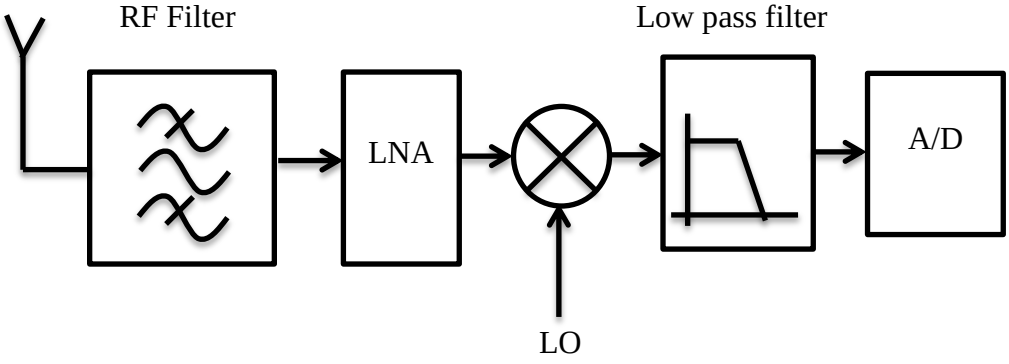


Fig. 1.1.2: RF receiver

A Low Noise Amplifier is an electronic device. A good LNA has a low noise figure (NF), a large enough gain and low power consumption. The total noise performance of the receiver depends on the Gain and Noise Figure of the LNA, as can be seen from the Friss equation which is reproduced here for convenience.

$$F_{cascade} = F_{stage1} + \frac{(F_{stage2}-1)}{Gain_{stage1}} + \frac{(F_{stage3}-1)}{Gain_{stage1}*Gain_{stage2}} + \cdots \quad 1.1$$

$$NF = 10log_{10}(F) \quad 1.2$$

LNA is used in various applications like ISM Radios, Cellular/PCS Handsets, GPS Receivers, Cordless Phones, Wireless LANs, Wireless Data, satellite communications etc. During reception of radio signal sent by satellite in a communication system, in the receiver section, second element after antenna is LNA. The receiver is the most power hungry block and the power consumption should be as low as possible. So, noise figure and power consumption are no less important issues than gain. While travelling through a medium it suffers due to various types of noise resulting in a very small signal to noise ratio. Due to this, direct reception of signal is not possible. Hence LNA is used to boost up the signal of desire energy from the weak information signal of required frequency.

1.2 Circuit Synthesis (Analog and RF)

The problem of circuit synthesis can be defined as selecting a circuit topology, allocating sizes to the composite components, and performing simulations on the sized circuit to check the correctness of the circuit with respect to the specifications that quantify it [2]. A physical layout is then produced based on the sizes of the components. Post-layout simulation with the newly created parasitic is performed to verify whether the layout meets the desired performance goals. Analog circuit synthesis has been a challenge for designers for decades. Analog circuit synthesis is considered an art and relies on the insight, experience and intuition of the designer to a large extent. We consider the salient features of Analog and RF synthesis below.

1.2.1 Analog Synthesis

Analog synthesis is a complex problem and demands a lot of time and effort. Analog behavioral synthesis is a research field and very little work has been done in that. In it the system's behavior is described using an Analog Hardware Description language (e.g. VHDL-AMS) and sized circuit net lists are produced [3]. On the other hand, considerable progress has been made in analog physical synthesis [4–6]. More details and references on work done in analog synthesis can be found in [7].

Analog Physical Synthesis:

Physical synthesis translates analog circuit schematics/net list to a full-custom layout. Important layout constraints like symmetry, matching is captured in this process. Figure 1.2.1 shows the various stages of analog physical synthesis.

1.2.2 RF Synthesis

RF circuit synthesis is very similar to analog synthesis and has an identical synthesis flow. However, RF circuits are highly prone to noise and distortion effects. Layout parasitics play a very important role. Layout symmetry, substrate coupling effects, transmission line effects etc. are some crucial factors which need special care. The following points illustrate some features which are typical of an RF synthesis flow.

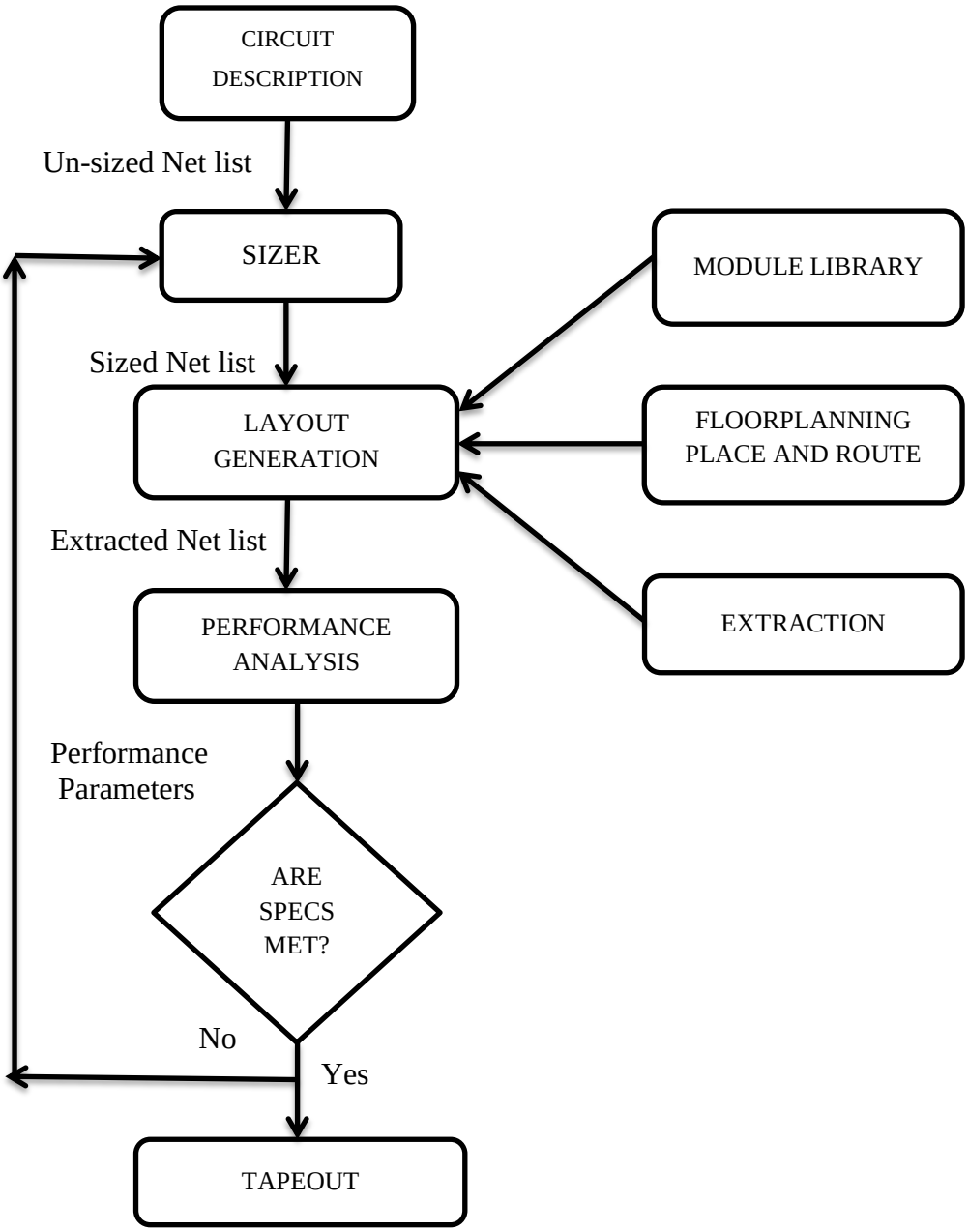


Fig 1.2.1: Analog Physical Synthesis Flow

Passive Component Extraction:

RF circuits invariably consist of on-chip passive components like resistors, capacitors, inductors and transistors, which are normally absent in low frequency analog circuits. Some of these components are not extracted by common extraction tools. Therefore specific extraction tools capable of performing this task need to be integrated in the synthesis flow.

Interconnect Parasitic Extraction:

As we move into deep submicron technologies the parasitic as associated with interconnects become significant. At high frequencies these parasitics can no longer be considered as lumped elements and full transmission line analysis needs to be performed.

Layout Features:

RF layouts need special care, as slight mismatch between elements can lead to noisy effects in the output. Guard rings need to be developed around sensitive components to reduce the substrate coupling effects.

1.3 LNA Architectures

In the designing of low noise amplifiers, the important goals are minimizing the noise figure of the amplifier, producing higher gain, low power consumption and producing stable 50 ohm input impedance [8]. To achieve all these goals different LNA architectures are available. Low noise amplifier is the first stage in the receiver design. Since, the operating frequency of LNA is in RF frequency band, the circuit should be as simple as possible, especially for the RF path. Otherwise, the circuit noise becomes too high. Moreover, if the circuit is too complicated, the parasitic effects may distort the amplified signal. Hence, there are several fundamental low noise amplifier topologies for single ended narrow band low power low voltage design, such as resistive termination common source, common gate, shunt series feedback common source, inductive degeneration common source, cascode inductor source degeneration.

Resistive termination common source

In resistive termination common source architecture, a resistor is added at the input side of the amplifier to get stable 50 ohm impedance, but will introduce some extra noise factor in the amplifier. Resistor termination common source topology adds noise to the LNA because of the resistor thermal noise. The resistive termination common source architecture is shown in Figure 1.3.1.

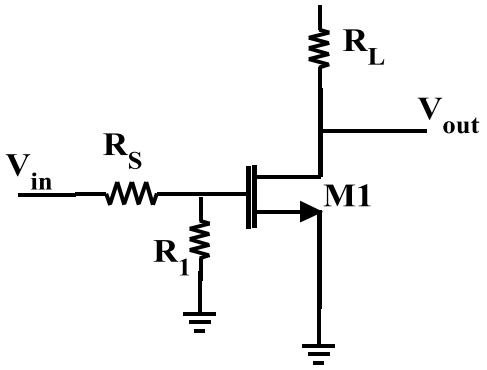


Fig. 1.3.1: Resistive termination common source

Common gate

In this architecture, common gate or common base configuration is used as the input termination. Common gate topology, the gain is less than 10.0 dB with very low power consumption. The common gate architecture is shown in Figure 1.3.2.

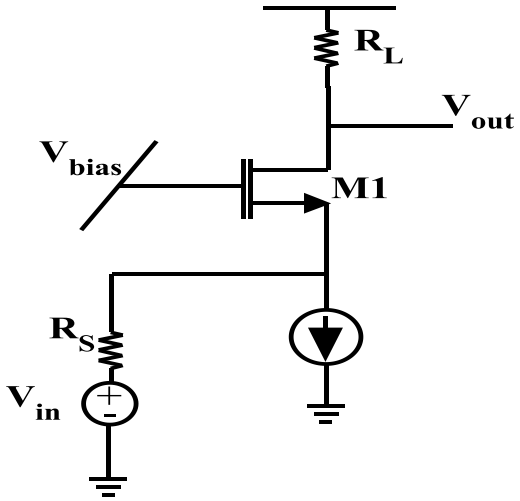


Fig. 1.3.2 : Common gate

Shunt series feedback common source

The shunt series feedback common source topology, it is difficult to trade off among gain, small noise figure and better input/output matching with very low power consumption. The shunt series feedback common source topology architecture is shown in Figure 1.3.3.

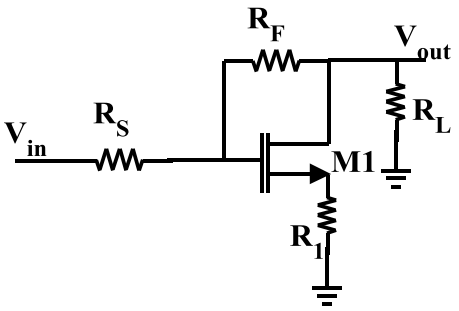


Fig. 1.3.3: Shunt series feedback common source topology

Inductive degeneration common source

Inductive degeneration architecture is most commonly used in GaAs MESFET amplifiers. These amplifiers use inductive source or emitter degeneration to provide a real term in the impedance. Inductive degeneration common source topology satisfies the specification in very low power consumption, but the isolation is not good enough compared to the cascade inductor source degeneration topology. The inductive degeneration common source topology architecture is shown in Figure 1.3.4.

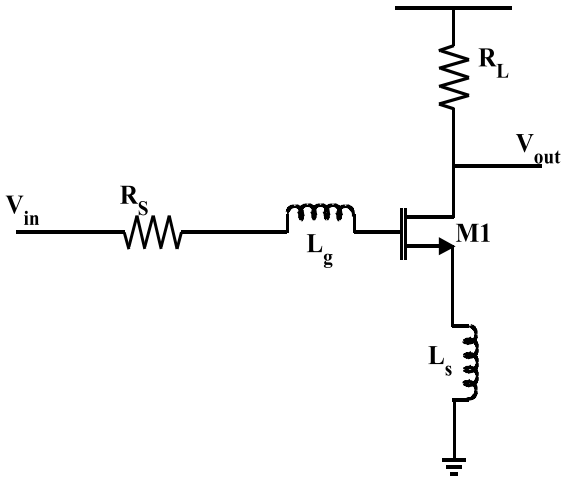


Fig. 1.3.4 : Inductive degeneration common source topology

Cascode inductor source degeneration

The Cascade inductor source degeneration topology satisfies the specification in good isolation, low noise amplifier performance with very low power consumption**.** The Cascade inductor source degeneration topology architecture is shown in Figure1.3.5.

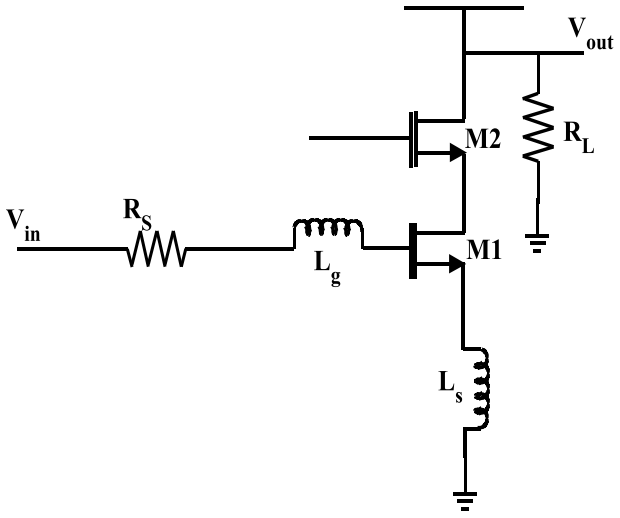


Fig. 1.3.5: Cascade inductor source degeneration topology

From the above all, the cascode inductor source degeneration topology provides higher gain with a low noise figure. The advantages and disadvantages of different kinds of LNA topologies are shown in Table 1.

Type	**Advantages**	**Disadvantages**
Resistive termination common source	Broad band amplifier	Adding the noise from the resistor
Common gate	The input impendence is equal to $1/g_m$. It is practical to get 50 Ω.	The impedance varies with the bias current.
Shunt series feedback common source	Broad band amplifier	Adding the noise from resistor
Inductive degeneration common source	The source and gate inductors make the input impendence 50 Ω. Not adding noise from the input.	The inductor is off chip at low frequency and low isolation.
Cascode inductor source degeneration	Isolation of input and output is good, higher gain, lower noise figure.	The inductor is off chip at low frequency.

Table 1: Advantages and disadvantages of LNA topologies

1.4 Literature review

Several topologies of the low noise amplifier are proposed in the literature. Somesh kumar and Dr. Ravi Kumar [9] have proposed a 1.8V and 2GHz Inductively Degenerated CMOS Low Noise Amplifier. Differential LNA block diagram and all other parameters discussed in this paper. Shaeffer and Lee [8] have proposed a CMOS low noise amplifier (LNA) which operates at 1.5V and 1.5 GHz frequency. Noise figure optimization techniques are also presented in this paper, with the detail discussion of the effects of induced gate noise in MOS devices. Goo et al. [10] presented a integrated low noise amplifier in which optimal noise performance is obtained by adjusting the source degeneration inductance. The effect of device geometry on NF is also presented in this paper. Molavi and Hashemi [11] have proposed a wideband CMOS LNA which is an extension of the narrowband power constrained simultaneous noise input matching LNA design technique. Qi and Jie [12] present a 1.5V, 0.18µm CMOS low noise amplifiers with differential topology thereby highlighting the benefits of this topology are also discussed in this paper. Muhamad and Nardin [13] presented the design for low noise amplifier at 0.18µm technology using power constrained noise optimization method. Fan et al. [14] have reported methods of noise reduction and linearity improvement of differential LNA. In this paper an inductor is connected at the gate of cascode transistor to reduce the noise. Andreani and Sjoland [15] present a technique for substantially reducing the noise of CMOS low noise amplifier implemented in the inductive source degeneration topology by taking into account the effect of gate induced current noise on the noise performance. Thus the efficacy of inductive source degeneration technique has been established beyond doubt. Xuan et al. Li [16] have proposed a 2.5 GHz differential CMOS LNA using 0.18µm CMOS process. In this two inputs and two outputs architecture are designed.

CHAPTER 2

Design steps and Fundamental analysis

This chapter specifies the parameters, target specifications for different topologies of low noise amplifiers (LNAs). Noise optimization techniques, design steps and analysis required for LNA is also discussed in this chapter.

2.1 Target Specifications

For the designing of a low noise amplifier (LNA) it seems appropriate to establish what the target specifications are. This is done in terms of a number of various parameters.

2. 1.1 S-Parameters

Linear networks and nonlinear networks operating with signals sufficiently small to cause the networks to respond in a linear manner can be completely characterized by parameters measured at the network terminals (ports) without regard to the contents of the networks [17]. Scattering parameters or S-parameters are important in microwave and RF design because they are easier to measure and work with at high frequencies as compared to other kinds of parameters such as the impedance (Z), admittance (Y) or hybrid (H) parameters. Scattering parameters are conceptually simple, analytically convenient, and capable of providing a great insight into a measurement or design problem [17].

Measuring most other parameters calls for the input and output of the device to be successively opened and short circuited [18]. This can be particularly difficult at RF frequencies where lead inductance and capacitance can make short and open circuits difficult to obtain. Scatter parameters are also called S-parameters. These parameters can be described by impedance (Z) and admittance (Y). At microwave frequencies S-parameters are very simple to measure. At high frequencies, as compared to other kind of port parameters, S-parameters are simpler and provide detailed information about modeling problem. S-parameters are defined in terms of the traveling waves which are scattered or reflected in the two port network when a circuit or network is connected to a transmission line with characteristic impedance Z_0.

To represent a two-port network at microwave frequencies, scattering parameters (S-parameters) can be used. S-parameters themselves ($S_{11}, S_{12}, S_{21}\ and\ S_{22}$) represent reflection and transmission coefficients of the two-port under certain "matched" conditions. S_{11} is the reflection coefficient and S_{21} is the transmission coefficient at port 1 when port 2 is terminated in a load whose impedance is equal to that of the transmission line characteristic impedance. Likewise S_{22} is the reflection coefficient and S_{12} is the transmission coefficient at port 2 when port 1 is terminated in a matched load. The two port network show as Figure 2.1.1.

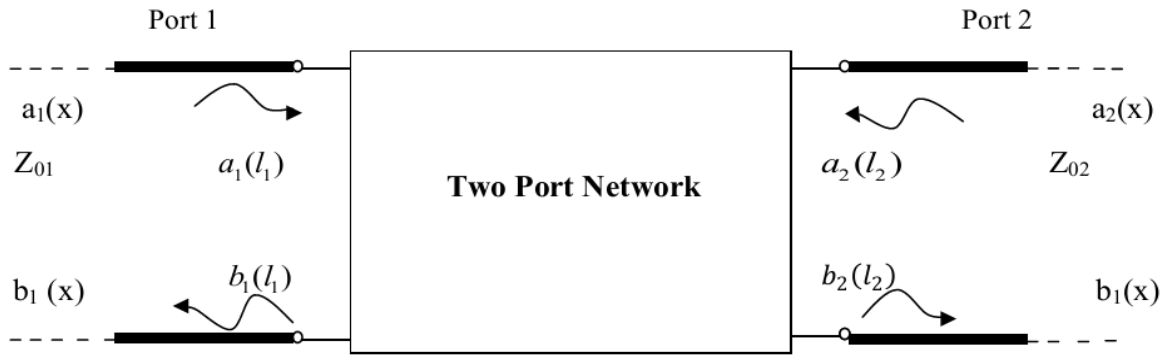


Fig. 2.1.1: Incident and reflected waves in a two-port network.

The LNA is characterized by the scattering matrix is

$$\begin{bmatrix} b_1(l_1) \\ b_2(l_2) \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad 2.1$$

Where $a_1(l_1)$ and $a_2(l_2)$ represent incident waves and $b_1(l_1)$ and $b_2(l_2)$ represent reflected waves.

Note that when the output port is terminated with $Z_L = Z_{02},\ a_2(l_2) = 0$. Therefore S_{11} and S_{21} can be defined as

$S_{11} = \frac{b_1(l_1)}{a_1(l_1)}$ and $a_2(l_2) = 0$ (input reflection coefficient; output port matched)

$S_{21} = \frac{b_2(l_2)}{a_1(l_1)}$ and $a_2(l_2) = 0$ (forward transmission coefficient; output port matched)

Note that when the input port is terminated with $Z_S = Z_{01},\ a_1(l_1) = 0$. Therefore S_{12} and S_{22} can be defined as

$S_{12} = \frac{b_1(l_1)}{a_2(l_2)}$ and $a_1(l_1) = 0$ (input reflection coefficient; input port matched)

$S_{22} = \frac{b_2(l_2)}{a_2(l_2)}$ and $a_1(l_1) = 0$ (reverse transmission coefficient; input port matched)

2.1.2 Gain

The gain of the device is its ability to amplify the amplitude or the power of the input signal. It is defined as the ratio of the output to the input signal and is often referred to in terms of decibels.

$$Voltage\ gain = 20\log(\frac{V_{out}}{V_{in}}) \quad 2.2$$

Power gain is generally defined as the ratio of the power actually delivered to the load to the power actually delivered by the source. Three power gains are commonly used in LNA design.

1. G_T, transducer power gain
2. G_P, operating power gain
3. G_A, available power gain

Transducer Power Gain:

Transducer power gain $G_T$is defined as the ratio between the power delivered to the load and the power available from the source

$$G_T = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{out}\Gamma_L|^2} \quad 2.3$$

The transducer gain expressions are too complex for manual design.

Operating Power Gain:

Operating power gain $G_P$is defined as the ratio between the power delivered to the load and the power input to the network.

$$G_P = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \quad 2.4$$

Available Power Gain:

Available power gain G_A is defined as the ratio between the power available from the network and the power available from the source.

$$G_A = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \quad 2.5$$

The power available from the source is greater than the power input to the LNA network, $G_P > G_T$. The closer the two gains are, the better the input matching.
Similarly, because the power available from the LNA network is greater than the power delivered to the load, $G_A > G_T$. The closer the two gains are, the better the output matching.

2.1.3 Noise Performance

The fundamental noise performance parameter is the Noise Factor (F), which is defined as the ratio of the total output noise power to the output noise due to input source. If the Noise Factor is expressed in decibels it is called the Noise Figure (NF). Another related and often talked about parameter in RF applications is the Signal-to-Noise Ratio (SNR), which is the ratio of the signal power and the noise power. Noise figure is commonly used to define extra noise generated by a circuit or system. Noise factor is defined as the ratio of the signal to noise power ratio at the input to the signal to noise power ratio at the output. The dB form of Noise factor is called Noise Figure.

$$NF = 10\log(F) = 10\log(\frac{SNR_{in}}{SNR_{out}}) \quad 2.6$$

$$= 10\log(\frac{\frac{Signal}{Noise_{in}}}{\frac{Signal}{Noise_{out}}}) = 10\log(1 + \frac{Noise_{amp}}{Noise_{in}}) \quad 2.7$$

Where

$Noise_{in}$ is the noise from the input stage

$Noise_{out}$ *is the noi*se at the output which consists of noise from amplifier

$\text{Noise}_{\text{amp}}$ plus the noise from $Noise_{in}$.

Noise figure sets the limitation on minimum signal strength, and linearity limits the maximum signal strength.

2.1.4 Linearity

Intermodulation distortion is the key limitation on the dynamic range performance of a small signal amplifier under large-signal conditions. Our goal here is to predict the nonlinear behavior, particularly third-order intermodulation distortion, as a function of device design, biasing, and impedance termination. The results can then be used in conjunction with the noise model of the device to optimize the dynamic range of an RF receiver [5]. The linearity of the LNA is another

concern that must be taken into account. Linear operation is crucial, particularly when the input signal is weak with a strong interfering signal in close proximity.

There are many measures of linearity, the most commonly used are the third-order intercept point (IP3) and the 1-dB compression point (P-1dB). IP3 shows at what power level the third-order intermodulation product is equal to the power of the first-order output. IIP3 and OIP3 are the input power and output power respectively, that corresponds to IP3. 1-dB compression point (P-1dB) shows at what power level the output power drops 1dB.

1-dB Compression point:

The 1-dB compression point is defined as the input power level in dBm at which the overall gain of amplifier is reduced by 1 dB from its maximum value. The 1-dB compression point is shown in Figure 2.1.2.

$$S_o(t) \approx a_1 S_i(t) + a_2 {S_i}^2(t) + a_3 {S_i}^3(t) \quad \ldots\ldots \tag{2.8}$$

$$\text{If} \quad S_i(t) = S_1 \cos \omega_1 t \tag{2.9}$$

$$S_o(t) = a_1 S_1 \cos \omega_1 t + a_2 {S_1}^2 cos^2 \omega_1 t + a_3 {S_1}^3 cos^3 \omega_1 t \tag{2.10}$$

$$= a_1 S_1 \cos \omega_1 t + a_2 (1/2) {S_1}^2 (\cos 2\omega_1 t + 1) + a_3 (1/4) {S_1}^3 (\cos 3\omega_1 t + 3 \cos \omega_1 t) \tag{2.11}$$

According to the definition, the 1 dB gain compression point is

$$20\log(a_1 S_1 + \frac{3}{4} a_3 {S_1}^3) = 20 \log(a_1 S_1) - 1dB \tag{2.12}$$

$$a_1 S_1 + \frac{3}{4} a_3 {S_1}^3 = \frac{a_1 S_1}{1.122} \tag{2.13}$$

$$0.1087 a_1 = -\frac{3}{4} a_3 {S_1}^2 \tag{2.14}$$

If a_3 is negative, then the magnitude of the required input voltage S_1

$$S_1 = V_{in} = \sqrt{0.145 \left|\frac{a_1}{a_3}\right|} \tag{2.15}$$

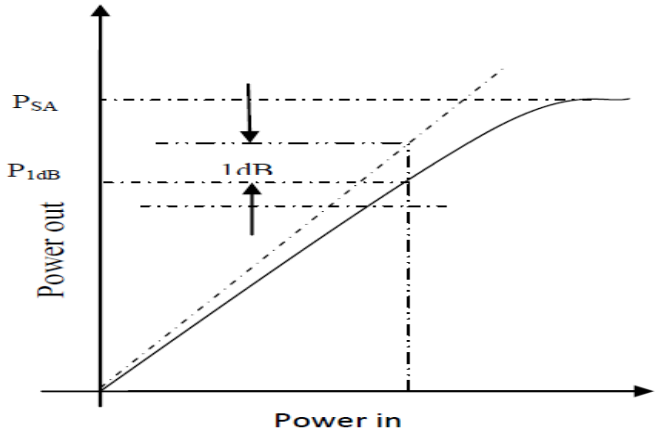


Fig. 2.1.2: 1 dB compression point

Third-order intermodulation distortion:

To measure the linearity of an RF block, the two-tone test is commonly used. One of the tones represents the desired RF signal and the other represents an adjacent channel interfering signal.

$$S_o(t) \approx a_1 S_i(t) + a_2 {S_i}^2(t) + a_3 {S_i}^3(t) \quad \ldots\ldots \tag{2.16}$$

$$\text{If} \quad S_i(t) = S_1 \cos \omega_1 t + S_2 \cos \omega_2 t \tag{2.17}$$

$$S_o(t) = a_1(S_1 \cos \omega_1 t + S_2 \cos \omega_2 t) + a_2 (S_1 \cos \omega_1 t + S_2 \cos \omega_2 t)^2 + a_3(S_1 \cos \omega_1 t + S_2 \cos \omega_2 t)^3 \quad \ldots\ldots \tag{2.18}$$

$$= a_1 S_1 \cos \omega_1 t + a_1 S_2 \cos \omega_2 t + a_2 S_1 S_2 \cos(\omega_1 + \omega_2)t + a_2 S_1 S_2 \cos(\omega_1 - \omega_2)t + \frac{3a_3 {S_1}^2 S_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3a_3 {S_1}^2 S_2}{4} \cos(2\omega_1 - \omega_2)t + \frac{3a_3 {S_2}^2 S_1}{4} \cos(2\omega_1 + \omega_2)t + \frac{3a_3 {S_2}^2 S_1}{4} \cos(2\omega_1 - \omega_2)t \tag{2.19}$$

The definition of IP3 is the input power in dBm where the fundamental output power and the third-order intermodulation output power are the same. Third-order intercept point is shown in Figure. 2.1.3. According to the definition, the equation of IP3 is

$$20\log(a_1 V_{in}) = 20 \log(\tfrac{3}{4} a_3 {V_{in}}^3) \tag{2.20}$$

$$a_1 V_{in} = \frac{3}{4} a_3 {V_{in}}^3 \tag{2.21}$$

$${V_{in}}^2 = -\frac{3}{4}\frac{a_1}{a_3} \tag{2.22}$$

$$V_{in} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{2.23}$$

By knowing either IP3 or the other can be estimated with the following rule- of- thumb formula

$$IP3 \approx P_{1dB} + 10dB \qquad 2.24$$

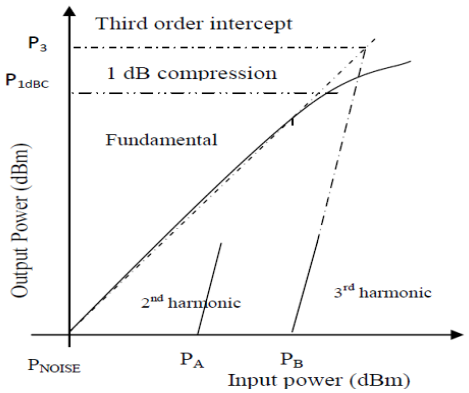


Fig..2.1.3 Third-order intercepts point

2.1.5 Stability

An important part of amplifier design is stability. In the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. The "Stability Factor and Measure" parameters are real functions of frequency and are available for 2-port networks only. These parameters aid in determining the stability of the 2-port network. If S_{12} of a device is not zero, a signal path will exist from the output to the input. This feedback path creates an opportunity for oscillation.

The stability factor is given as

$$K=\frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \qquad 2.25$$

Where

$$|\Delta| = S_{11}S_{22} - S_{12}S_{21} \qquad 2.26$$

When $K > 1$ and $|\Delta| < 1$, the circuit is unconditionally stable.

2.2 Selection of appropriate circuit components

Because MOSFETs, spiral inductors and capacitors are often used in LNA circuit, the accurate RF models are very important to predict the silicon performance of gigahertz circuits. The characteristic of transistor in low frequency is different from the one in high frequency. The parasitic effects of transistor should be considered in circuit design, which are not included in the low frequency circuit design. So the transistor model for low frequency design is quite different with the model for high frequency design. Moreover in high frequency, the inductance and Q value varies with the operating frequency and capacitor also has parasitic effects. Spectre-RF simulator of Cadence is used for the design of various topologies of LNA. The analog Lib library in Cadence is used for selecting other active and passive components.

2.2.1 MOSFET RF Models

MOSFET models, especially the RF MOSFET models are required to predict the silicon performance accurately, such as sub-circuit short channel MOSFET models for RFIC designs. In the sub-circuit models, MOSFET is divided into two parts, an intrinsic part and an extrinsic part. The intrinsic part represents the main active part of the device, which can be any compact model, such as Berkeley Short-Channel IGFET Model (BSIM). However, the extrinsic part consists of most of the parasitic elements, including all the terminal access series resistance, gate resistance, overlap and junction capacitance, and substrate network.

The UMC_18_CMOS library in Spectre RF contains various MOSFET models given in the appendix A From these MOSFETs, N_L18W500_18_RF device is used for the designing of LNAs. The length of this transistor is constant 180.0nm and finger number is variable. The range of finger number is 5-21. The maximum allowable width of N_L18W500_18_RF in Spectre RF is 105µm (21×5). Two or more transistors are used in parallel for the bigger transistors. For the PMOSFET, P_L18W500_18_RF device is used for designing of LNAs.

Different types of RF MOSFET are shown below.

- N_L18W500_18_RF - 1.8 volt variable finger RF NMOS transistor
- N_L34W500_33_RF - 3.3 volt variable finger RF NMOS transistor
- N_PO7W500_18_RF - 1.8 volt variable length RF NMOS transistor
- N_PO7W500_33_RF - 3.3 volt variable length RF NMOS transistor

• P_L18W500_18_RF - 1.8 volt variable finger RF PMOS transistor
• P_L34W500_33_RF - 3.3 volt variable finger RF PMOS transistor
• P_PO7W500_18_RF -1.8 volt variable length RF PMOS transistor
• P_PO7W500_33_RF - 3.3 volt variable length RF PMOS transistor

2.2.2 Inductors RF Models

Spiral inductors with reasonable Q and self-resonant frequency are widely used in the RFIC designs, such as fully integrated LNA, oscillator and impedance matching network. They are proved to be most difficult passive components to be implemented on chip. Circular square spiral inductor is defined by side length, wire width, wire space and number of turns. The UMC_18_CMOS library in Spectre RF contains the inductor model given in the appendix A. L_SLCR20K_RF inductor model is used for the designing of LNAs. It is a three terminal inductor. Model range of turn numbers is 1.5-5.5 and the model range of width is 6 µm-20 µm. The model range of diameter is 126.0 µm-238.9 µm. As the turn number decreases the inductance also decreases. The maximum value of inductance is 14.054 nH and if I want more than 14.054 nH then two inductors in series are used.

2.2.3 Capacitors RF Models

Capacitors are another important passive components widely used in RF circuit design, such as impedance matching and DC block. The usage of a capacitor is primarily dependent upon the characteristics of its dielectric. The dielectric's characteristics also determine the voltage levels and the temperature extremes at which the device may be used. The UMC_18_CMOS library in Spectre RF contains various capacitors models given in the appendix B. From these capacitors, MIMCAPM_RF device is used for the designing of LNAs. It is a three terminal capacitor. The model range of width and length is 10-70 µm and range of ratio is =<6 and >=1. The maximum value of this capacitor is 5.047 pF and minimum value is 103.00f.

2.2.4 Resistors RF Models

Resistance is the property of a material that determines the rate at which electrical energy is converted into heat energy for a given electric current. At very high frequencies and with low-value resistors (under 50 ohms), lead inductance and skin effect may become noticeable. The UMC_18_CMOS library in Spectre RF contains various resistors models given in the appendix B. From these capacitors, RNNPO_RF device is used for the designing of LNAs. It is a three terminal resistor. The model range of width is 2-10 µm. The model range of length is 2-100 µm and range of ratio is <=10 and >=1. The maximum value of resistance is 1.205465KΩ and minimum value is 136.6264 Ω.

Different types of Resistor RF models are shown below.

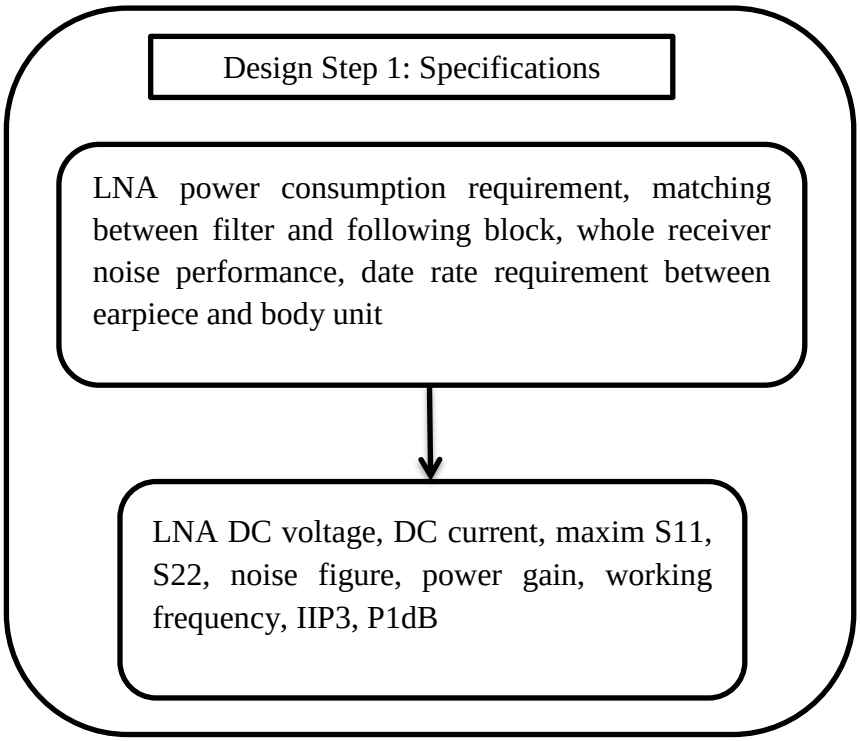
• RNHR_RF - RF High resistive poly resistor

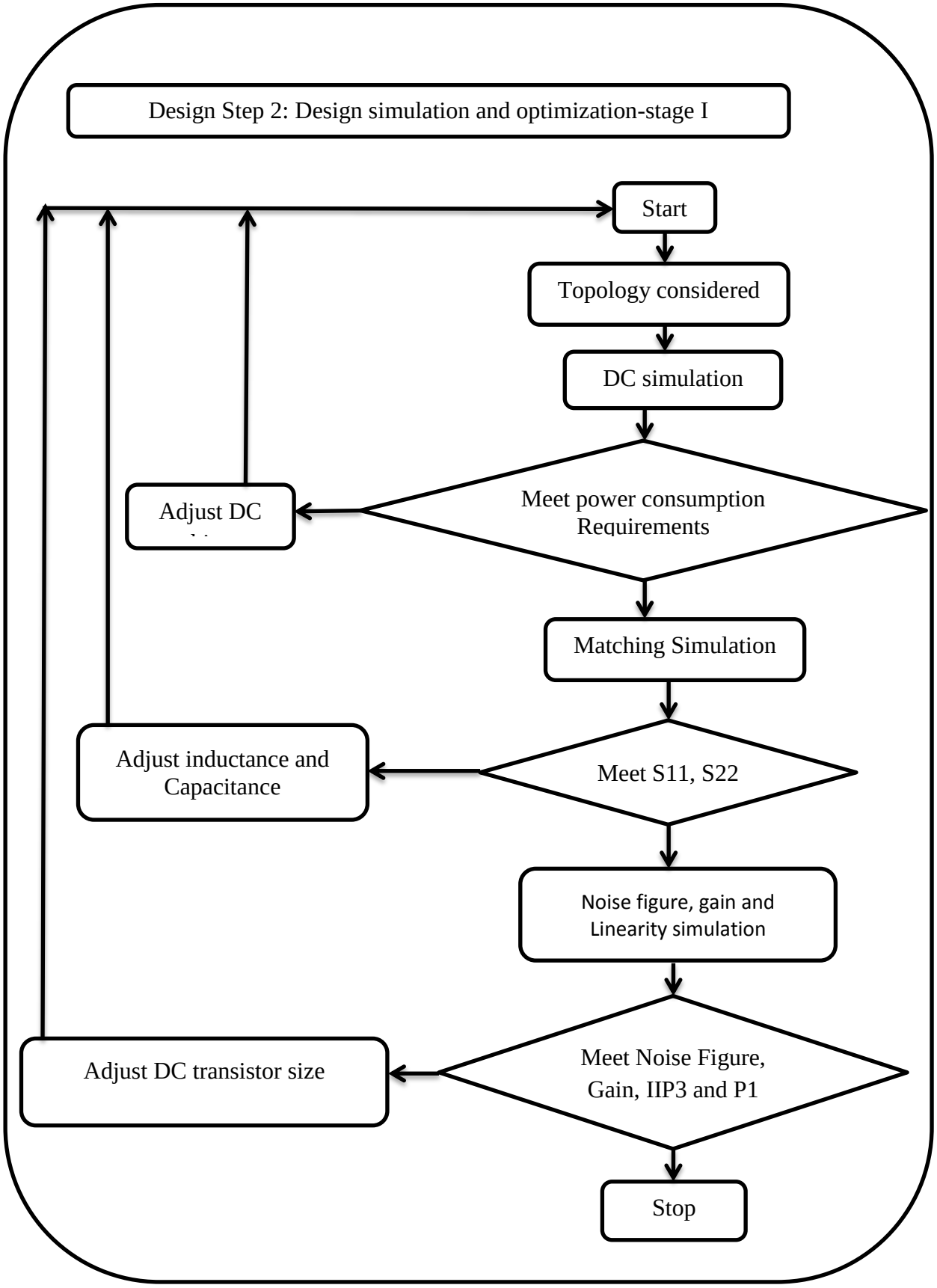
• RNNPO_RF - RF N+ poly resistor w/o silicide

• RNPPO_RF - RF P+ poly resistor w/o silicide

2.3 LNA Design and Optimization Steps

The design and optimization steps followed in the design of presented LNAs are mentioned below. For each step, the design flow is shown in Figure 2.3.1.




Design Step 2: Design simulation and optimization-stage I
Start
Topology considered
DC simulation
Meet power consumption Requirements
Adjust DC
Matching Simulation
Meet S11, S22
Adjust inductance and Capacitance
Noise figure, gain and Linearity simulation
Meet Noise Figure, Gain, IIP3 and P1
Adjust DC transistor size
Stop

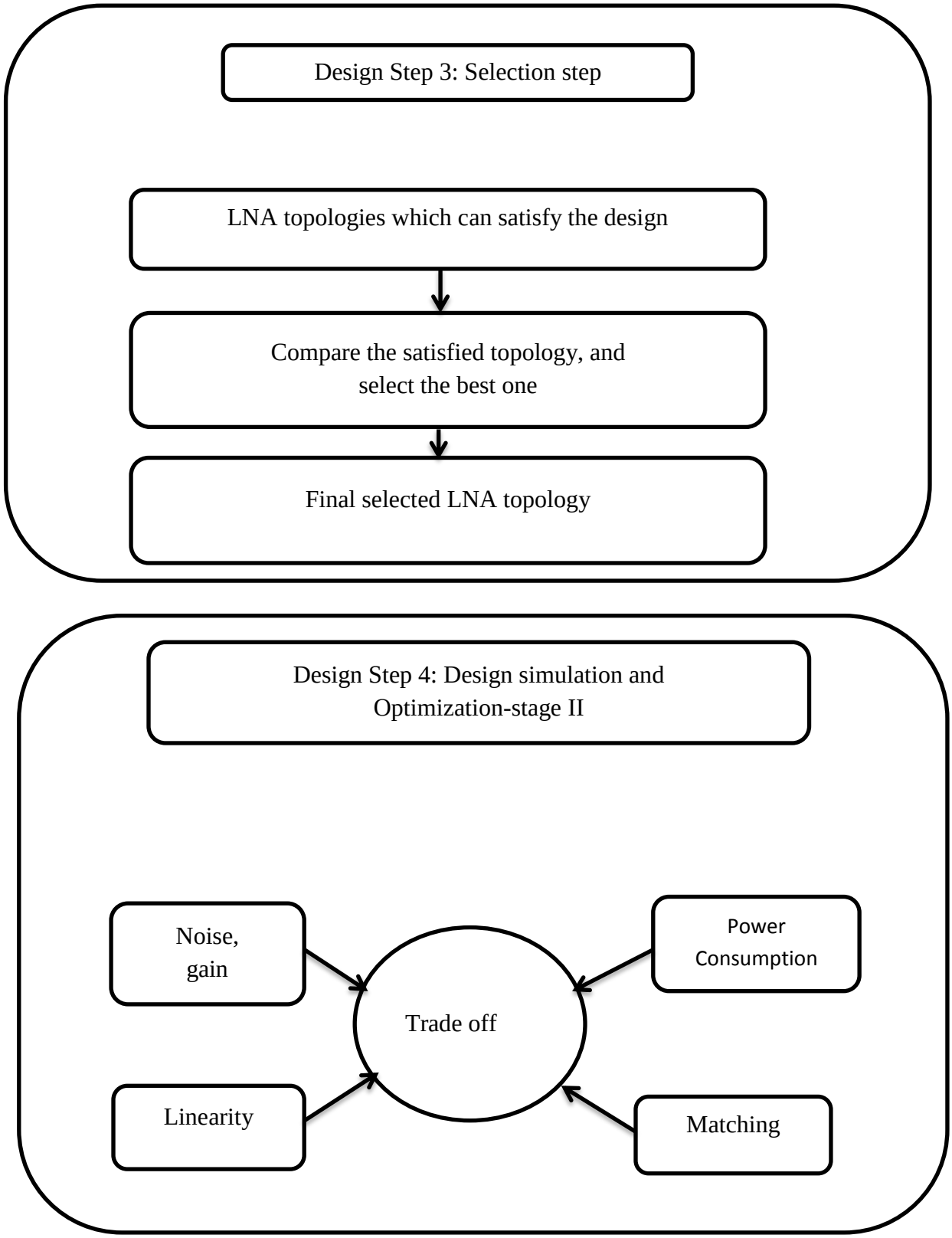


Fig. 2.3.1: Design steps of LNA

2.4 Analysis required

S-Parameters (SP), Periodic Steady State Analysis (PSS), P_{noise} and DC analysis available in Spectre RF is used by me to simulate the parameters of LNA. Usually there is more than one method available to simulate the desired parameter. The procedure that takes less simulation time is used by me. The various analyses required are given below

2.4.1 DC Analysis

The DC analysis is used to calculate the power consumption. First to set the power consumption requirement, we have to adjust the DC bias resistor, transistor sizes and source degenerated inductor. The DC current was found with the help of DC simulations.

2.4.2 S-Parameter Analysis

The S-Parameter analysis is used to compute scattering and noise parameters for 2-port circuits that exhibit frequency translation. S-Parameter analysis is used for small-signal and linear noise analyses, where the circuits are linearized around the DC operating point. Such circuits include LNAs, mixers, samplers and other similar circuits. SP analysis also calculates noise parameters in frequency-converting circuits. SP computes noise figure, input referred noise, equivalent noise parameters, and noise correlation matrices. For the SP analysis, I required to specifying the input and output ports and the range of sweep frequencies. After setting SP analysis for the LNA, I can extract and plot the following gain and matching parameters measurements.

- S11, input reflection coefficient
- S21, forward gain
- S12, reverse gain
- S22, output reflection coefficient
- GT, transducer power gain
- GP, operating power gain
- GA, available power gain

By setting the input and output noise port, I can plot NF and NF_{min} with respect to frequency. The Stern stability factor K_f and Δ can be plotted with respect to frequency.

2.4.3 PSS and P_{noise} Analysis

Use the PSS and P_{noise} analyses for large-signal and nonlinear noise analyses, where the circuits are linearized around the periodic steady-state operating point. As the input power level increases, the circuit becomes nonlinear, the harmonics are generated and the noise spectrum is folded. Therefore, PSS and P_{noise} analyses are used by me. When the input power level remains low, the NF calculated from the P_{noise}, Noise, and SP analyses should all match. Spectre RF simulation uses a technique called the shooting method to implement PSS analysis. This method is an iterative, time-domain method that finds an initial condition that directly results in a steady-state. It starts with a guess of the initial condition. By the PSS analysis, I can determine the voltage gain of the low noise amplifier. The P_{noise} analysis summary shows you the contributions of different noise sources in the total noise. This is very powerful feature to focus the effort to improve the noise performance of the device which contributes the maximum noise. First PSS analysis is required for the P_{noise} analysis. After the P_{noise} analysis, I can plot the noise figure with respect to frequency.

2.4.4 PSS

After the PSS analysis with swept input power level, plot the output power against the input power level. This plot shows the 1 dB compression point. A two-tone test is used to measure an IP3 curve where the two input tones are ω_1 and ω_2. Since the first-order components grow linearly and third-order components grow cubically, they eventually intercept as the input power level increases. The IP3 is defined as the cross point of the power for the 1st order tones, ω_1 and ω_2, and the power for the 3rd order tones, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, on the load side. Two input frequencies are chosen for the swept PSS. The IPN curves option is selected from the Affirma window. Then IP3 and P1 dB point can be plotted.

CHAPTER 3

Design of LNA

The first stage of a receiver is typically a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages. This work presents the design of an inductively source degenerated CMOS differential cascode Low Noise Amplifier (LNA) and without source degenerated CMOS differential cascode Low Noise Amplifier (LNA) operating at 2 GHz frequency.

3.1 Source Degenerated LNA

The L_s is the degeneration inductor. We can adjust the inductor to fit the variation of f_T, but f_T is so large that the value of the inductor will be less than 0.4nH, which is difficulty to be implemented on chip [19] is shown in fig. 3.1.1 and small signal equivalent circuit of Source Degenerated LNA is as shown in fig. 3.1.2.

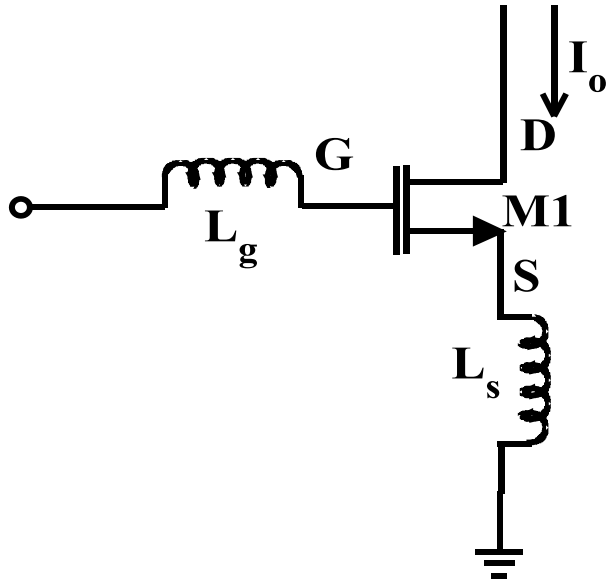


Fig. 3.1.1. Source Degenerate LNA

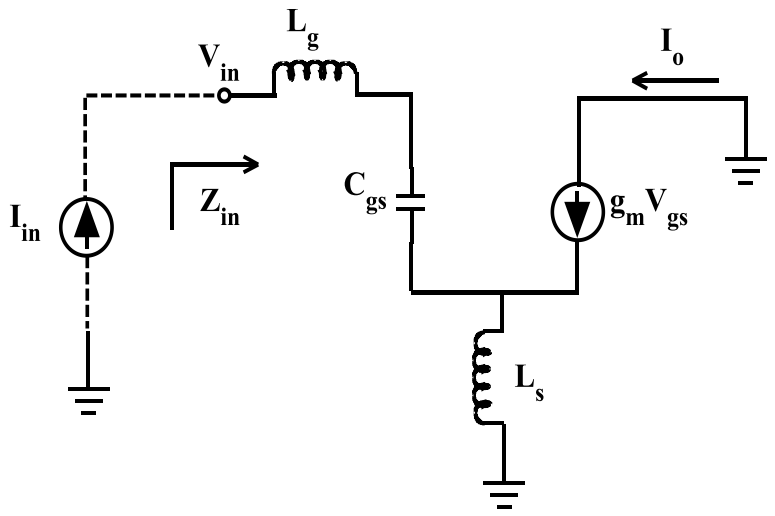


Fig. 3.1.2.Small signal equivalent circuit of Source Degenerated LNA.

Writing KCL and KVL equations for Source degeneration LNA

$$I_0 = g_m V_{gs} = I_{in} \times \frac{1}{sC_{gs}} g_m = \frac{g_m}{sC_{gs}} I_{in} \quad 3.1$$

$$\mathrm{V_{in}} = [\mathrm{s(L_g + L_s)} + \frac{1}{\mathrm{sC_{gs}}}]\mathrm{I_{in}} + \mathrm{I_0 sL_s} \quad 3.2$$

Solving (1) and (2)

$$Z_{in} = \frac{V_{in}}{I_{in}} = s(L_G + L_S) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \quad 3.3$$

$$Z_{in}(j\omega) = j\left[(L_g + L_s)\omega - \frac{1}{\omega C_{gs}}\right] + \frac{g_m L_s}{C_{gs}} \quad 3.4$$

Matching occurs when $Z(j\omega_0) = R_s$. R_s is the resistor, which is associated in the input voltage source. That is

$$(L_G + L_s)\omega_0 = \frac{1}{\omega_0 C_{gs}} \quad 3.5$$

$$\omega_0{}^2 = \frac{1}{(L_G + L_S)C_{gs}} \quad 3.6$$

and

$$R_s = \frac{g_m l_s}{C_{gs}} \quad 3.7$$

$$L_G = \frac{1}{\omega_0{}^2 C_{gs}} - L_s \quad 3.8$$

and

$$L_S = \frac{1}{\omega_0{}^2 C_{gs}} - L_G \quad 3.9$$

3.2 Capacitor(C_x) is added between the gate and source of Source degenerated LNA

The capacitor (C_x) is added between the gate of the MOSFET and source of MOSFET is as shown in fig. 3.2.1 and small signal equivalent circuit of Source Degenerated LNA is as shown in fig. 3.2.2. The use of C_x capacitance is to increase the Source Degenerated inductor value, increase the noise figure, and reduce the power gain of LNA.

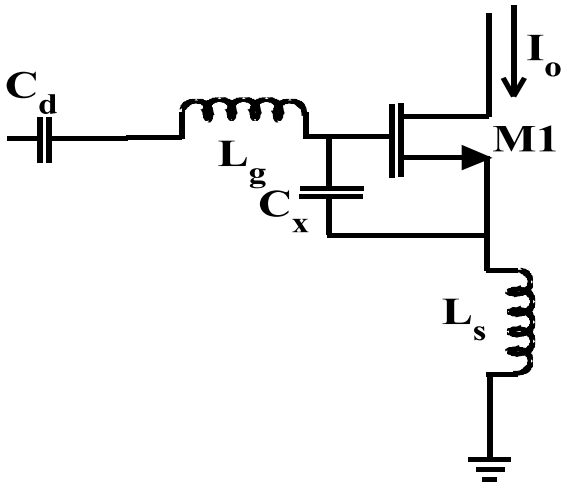


Fig. 3.2.1. Capacitor C_x is added between the gate and source of Source Degenerated LNA

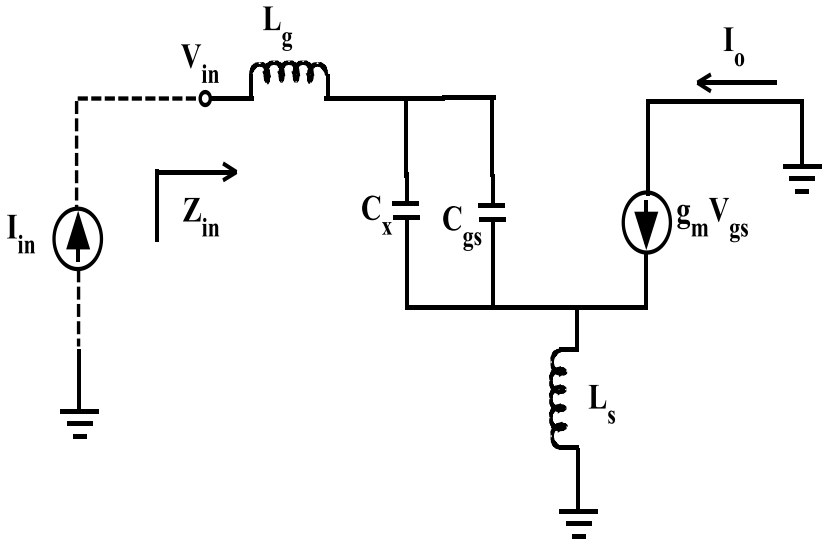


Fig. 3.2.2. Small signal equivalent circuit of capacitor C_x is added between the gate and source of Source Degenerated LNA.

Writing KCL and KVL equations for Source degeneration LNA

$$I_0 = g_m V_{gs} = I_{in} \times \frac{1}{sC_{gs}+sC_x} g_m = \frac{g_m}{sC_{gs}+sC_x} I_{in} \quad 3.10$$

$$\mathrm{V_{in}} = [\mathrm{s(L_g + L_s)} + \frac{1}{sC'_{gs}}]\mathrm{I_{in+} I_0 s L_s} \quad 3.11$$

Where

$$C'_{gs} = C_{gs} + C_x \quad 3.12$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = s(L_G + L_S) + \frac{1}{sC'_{gs}} + \frac{g_m L_s}{C'_{gs}} \quad 3.13$$

$$Z_{in}(j\omega) = j\left[(L_g + L_s)\omega - \frac{1}{\omega C'_{gs}}\right] + \frac{g_m L_s}{C'_{gs}} \quad 3.14$$

Matching occurs when $Z(j\omega_0) = R_s$. R_s is the resistor, which is associated in the input voltage source. That is

$$(L_G + L_s)\omega_0 = \frac{1}{\omega_0 C'_{gs}} \quad 3.15$$

$$\omega_0{}^2 = \frac{1}{(L_G+L_S)C'_{gs}} \quad 3.16$$

And

$$R_s = \frac{g_m l_s}{C'_{gs}} \quad 3.17$$

$$L_G = \frac{1}{\omega_0{}^2 C'_{gs}} - L_s \quad 3.18$$

and

$$L_S = \frac{1}{\omega_0{}^2 C'_{gs}} - L_G \quad 3.19$$

3.3 Input impedance matching

S-parameter analysis was used to measure the input impedance of the LNA. The input impedance (Z_{in}) is measured from the plot of S_{11}, where S_{11} represents the input reflection coefficient with the output properly terminated. The capacitor C_x is added between the gate of the MOSFET and source of MOSFET is as shown in fig. 3.3.1. The use of C_x capacitance is to increase the Source Degenerated inductor value, increase the noise figure, and reduce the power gain of LNA. The conditions for input impedance matching Z_{in} and the expression for the resonant frequency ω_0 are shown in (11).

L_s and L_g together with the capacitance C_{gs} and C_x form an input impedance matching network. The input impedance matching Z_{in} = 50Ω.

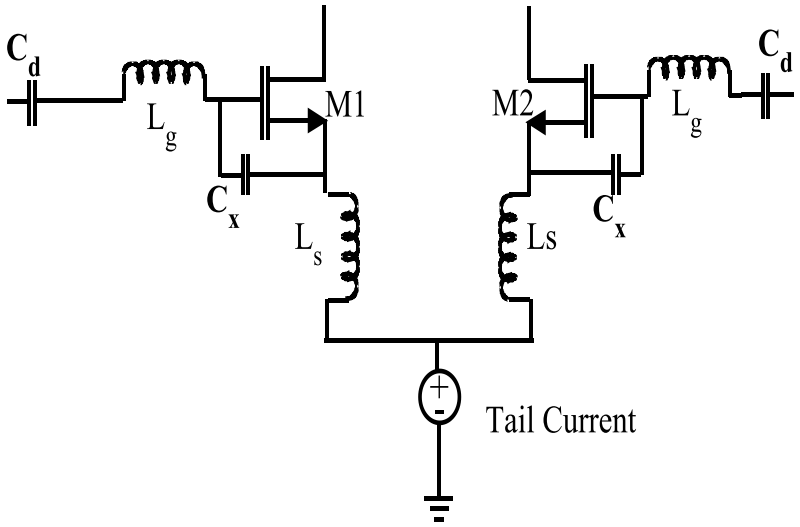


Fig. 3.3.1. Input impedance matching

The gate inductance L_g is used to set the resonance once L_s is chosen to satisfy the criterion of a 50Ω pure resistance [20].

$$Z_{in}(s) = \frac{1}{sC'_{gs}} + s\left(L_g + L_s\right) + \frac{g_m}{C'_{gs}} L_s \quad 3.20$$

$$C'_{gs} = C_{gs} + C_x \quad 3.21$$

3.4 Differential LNA design

Differential circuits are an important part of integrated circuit design because they offer several important advantages over single-ended circuits [21]. The first important advantage is the differential LNA offers a stable reference point. With any type of circuit, the measured values are always taken with respect to a reference. In the differential LNA the measured results of one-half circuit are always taken with respect to other half circuit. Another significant and relevant benefit of using a differential circuit is noise reduction. The inductively source degenerated differential cascode LNA can be considered as a CS-CG two stage LNA.

To supply a differential signal to each LNA input, an „ideal" balun (balanced to unbalanced) transformer has been used (The two AC sources each set to some voltage and opposite polarity can be used). In addition another balun is used on the amplifier output to re-combine the signal to allow the voltage gain to be simulated. When balun is not used at the output then two ports are required at the output. The parameters selected for two ports differential LNA is given below in table 2

An additional inductor L_{add} combined with the capacitive cross-coupling technique is applied to the cascode transistor of the differential LNA to reduce the noise and increase the gain. Inter-stage inductor form impedance match network between input stage and cascoded stage boost gain, reduce the noise figure and affects the input match condition.

In order to make the differential LNA circuit, two single-ended circuits built, where each transistor and circuit component has a complimentary transistor or component. The positive input voltage is measured at the gate of one of the half-circuit CS amplifiers, while the negative input voltage is measured at the gate of the other half-circuit. The overall output of the LNA is measured between the sources of each half-circuit.

Parameter	Port 1	Port 2
Cell name	Psin	Psin
Frequency Name	f1	
Resistance	50Ω	50Ω
Port number	1	2
DC voltage	0.7V	
Source type	Sine	
Amplitude (dBm)	Pr	
Frequency	Fr	
AC magnitude	1 V	

Table 2: Port parameters of Differential LNA

3.4.1 Capacitor cross-coupled with inductively source degenerated differential LNA

A capacitor cross-coupled with inductively source degenerated differential LNA design circuit as shown in fig. 3.4.1 and schematic of capacitor cross-coupled with inductively source degenerated differential LNA circuit shown in fig. 3.4.2. The use of source degeneration is the effects of the gate induced current noise on the noise performance and the total output noise is strongly reduced by inserting a capacitance of appropriate value in parallel with the amplifying MOS transistor of the LNA. It results very low noise figure and very low power consumption.

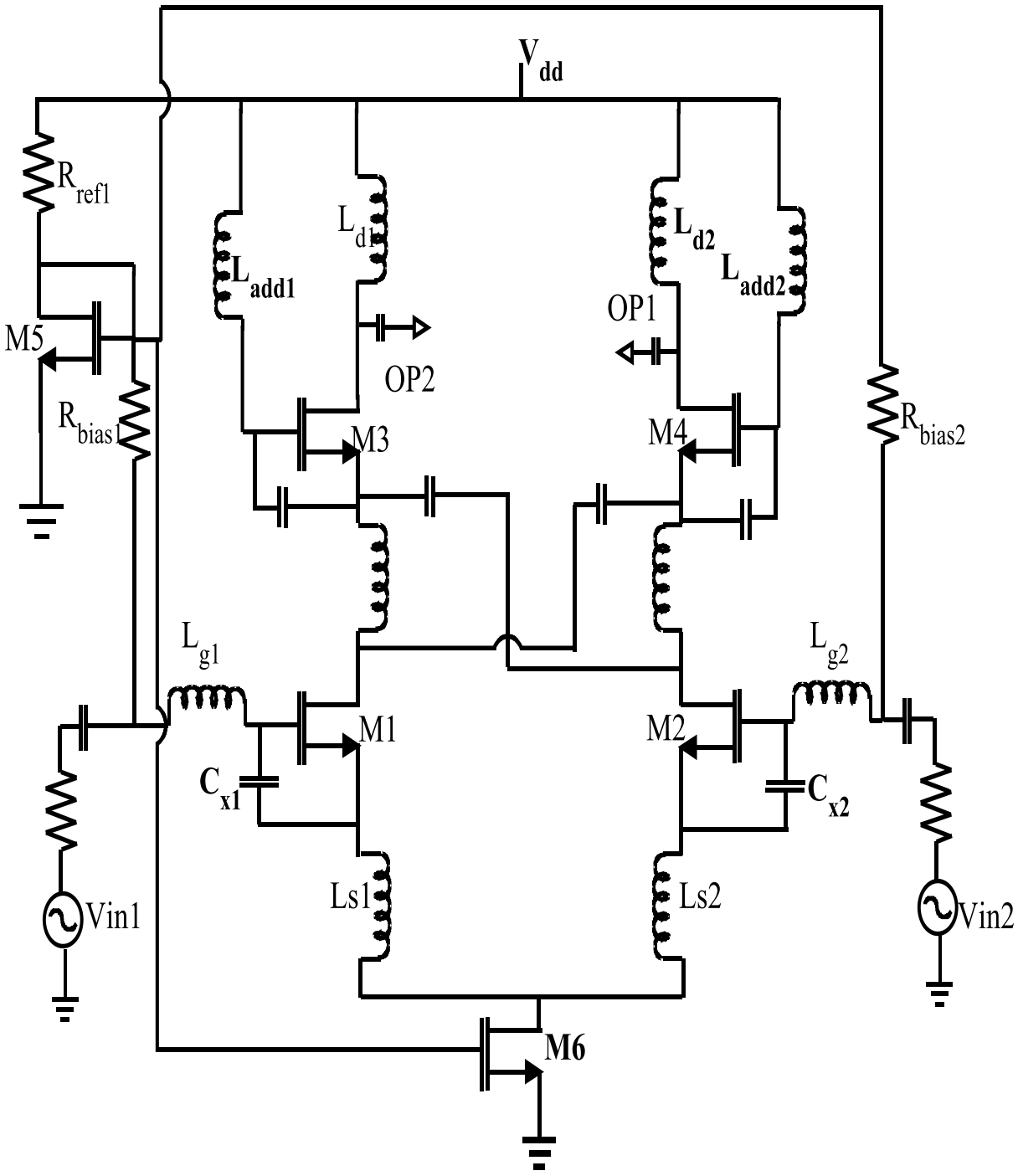


Fig. 3.4.1 Capacitor cross-coupled with inductively source degenerated differential cascode LNA design

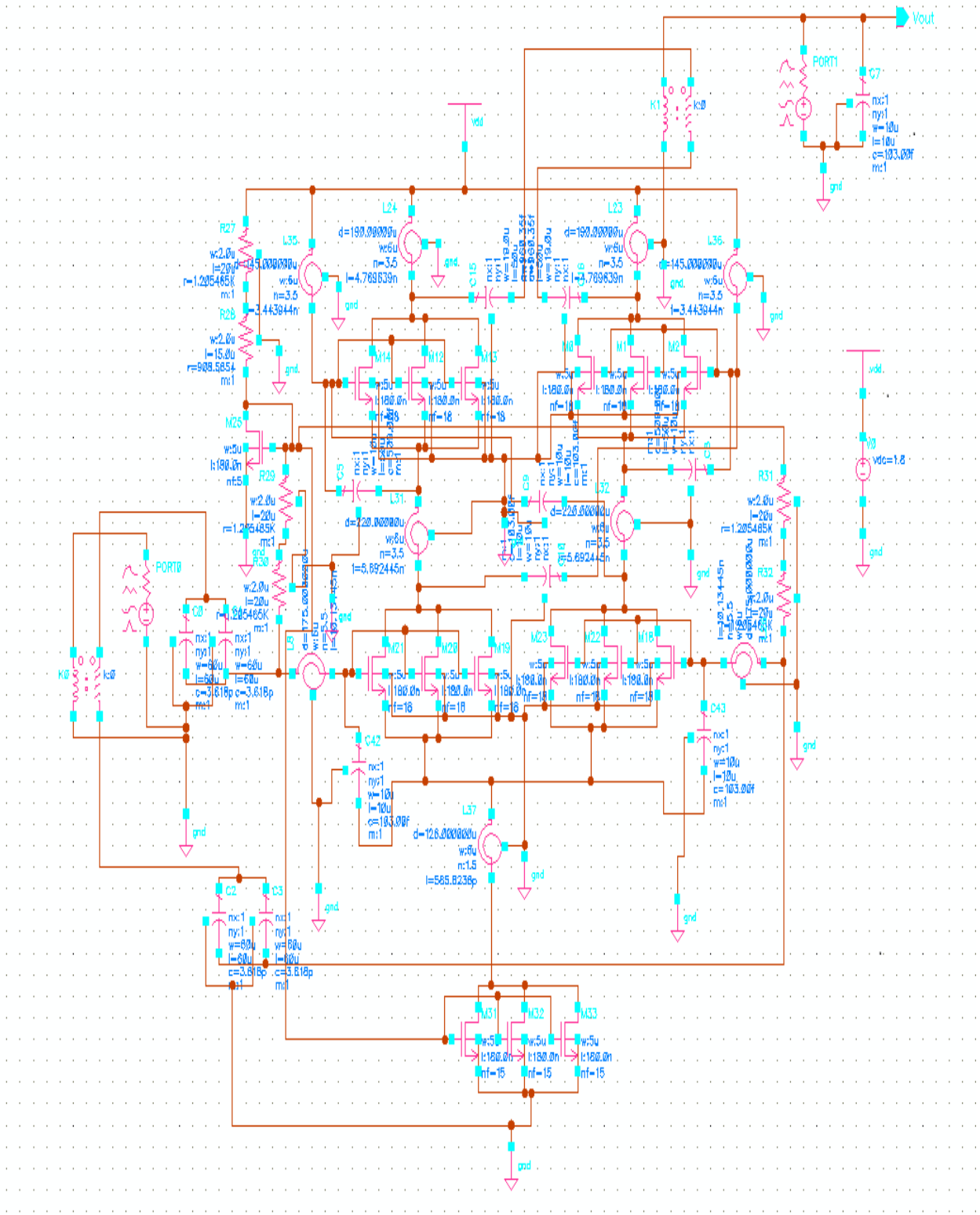


Fig. 3.4.2. Schematic of capacitor cross-coupled with inductively source degenerated differential cascode LNA design

3.4.2 Capacitor cross-coupled without inductively source degenerated differential LNA

A capacitor cross-coupled without inductively source degenerated differential LNA design circuit as shown in fig. 3.4.3 and schematic of capacitor cross-coupled without inductively source degenerated differential LNA circuit shown in fig. 3.4.4. The dis-advantages of without source degenerated differential LNA are linearity decreases and noise increases.

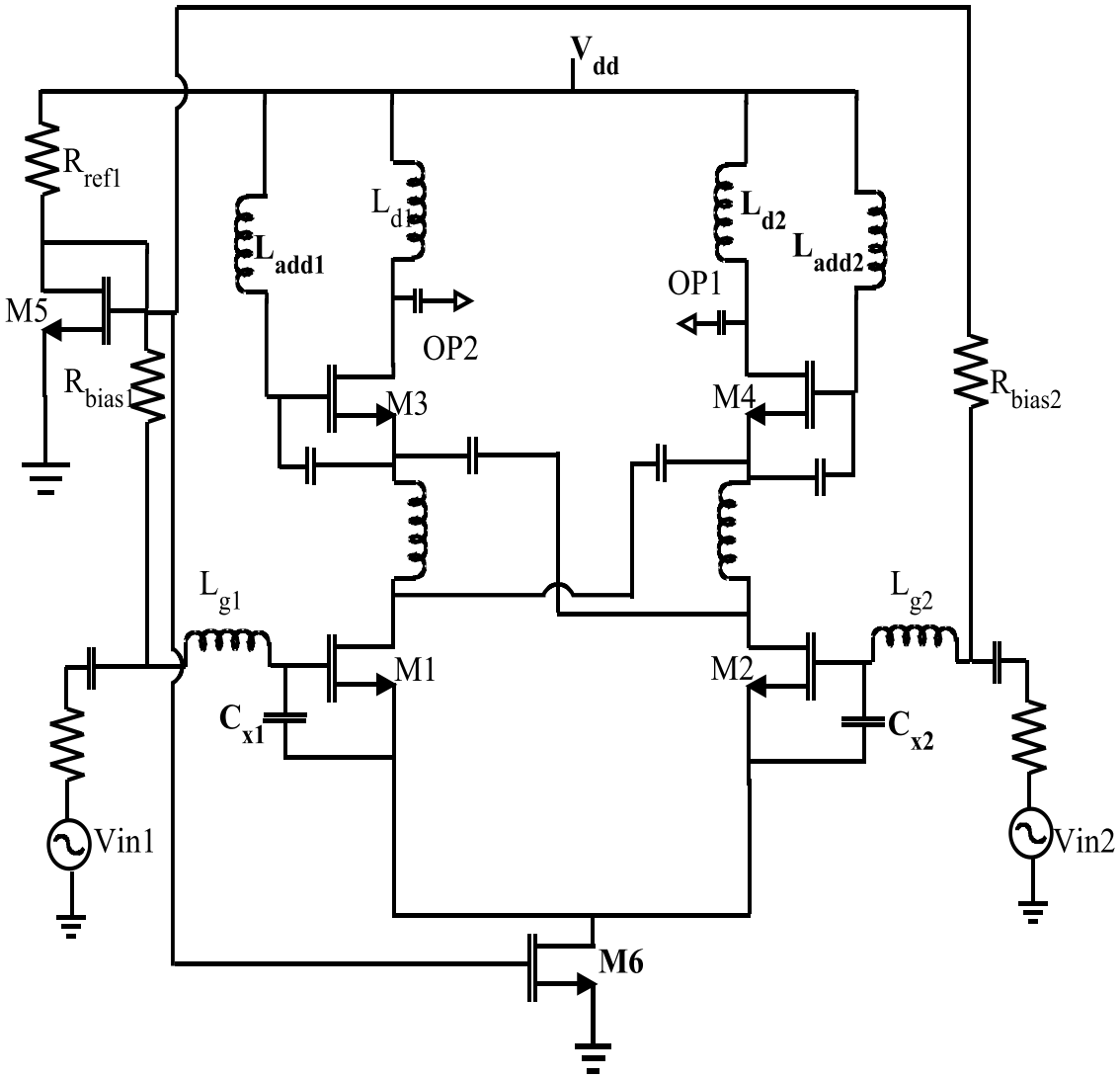


Fig 3.4.3 Capacitor cross-coupled without inductively source degenerated differential LNA design circuit

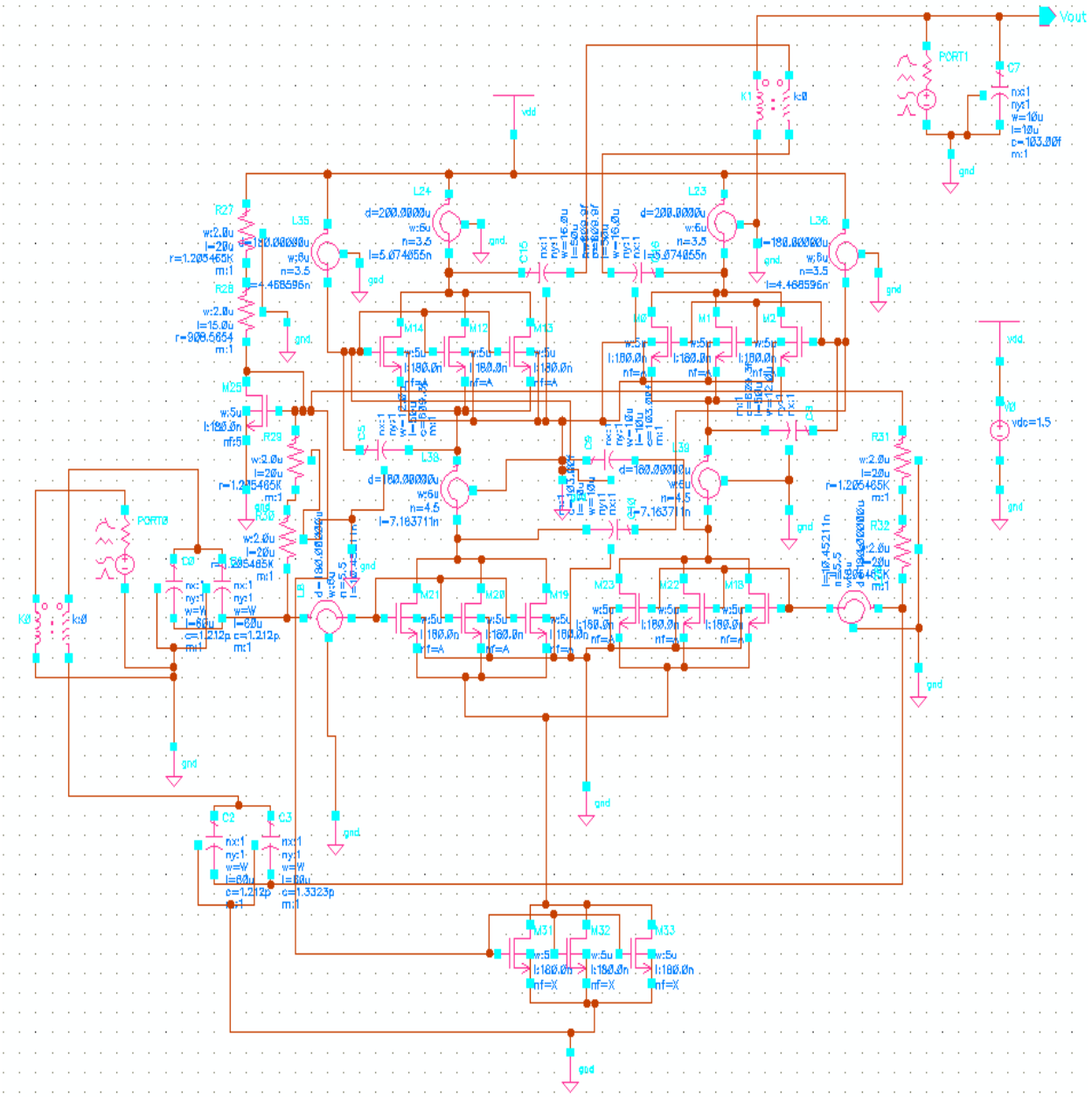


Fig. 3.4.4. Schematic of capacitor cross-coupled without inductively source degenerated differential LNA design circuit

CHAPTER 4

Simulations

With the differential circuit designed, simulations could be used to verify that the circuit was meeting specifications as designed. Simulations were performed using DC, Periodic noise, scattering parameters (S-parameters) and Periodic Steady State (PSS) analyses. These analyses allowed the circuits operation to be simulation including operating points of the transistors, noise performance, gain, linearity, input impedance, power gain among others.

We have simulated our design using Cadence spectre_RF tool on UMC 0.18 μm technology. The RF transistor models, inductor models, capacitor models and resistor models are provided by library UMC_18_CMOS in 0.18 μm technology. Cadence EDA tools used are Virtuoso for Schematic Editing and Spectre for Simulation.

4.1 Simulation wave forms of with inductively source degenerated differential LNA

The various simulation iterations are performed on the capacitor cross-coupled with source degenerated differential LNA circuit to meet design requirements. The simulation wave forms of capacitor cross-coupled with inductively source degenerated differential LNA operating at 2GHz frequency with supply voltage 1.8 V.

4.1.1 Voltage gain

The voltage gain was measured from the AC analysis as the difference in decibels between the output voltage and input voltage. It can be seen from the below graphs (Fig. 4.1.1) that the differential LNA has a voltage gain of approximately 16.95 dB at 1.8 V supply voltage, a center frequency of 2 GHz. This gain is sufficient to amplify any weak signal, but the gain will drop when layout is performed.

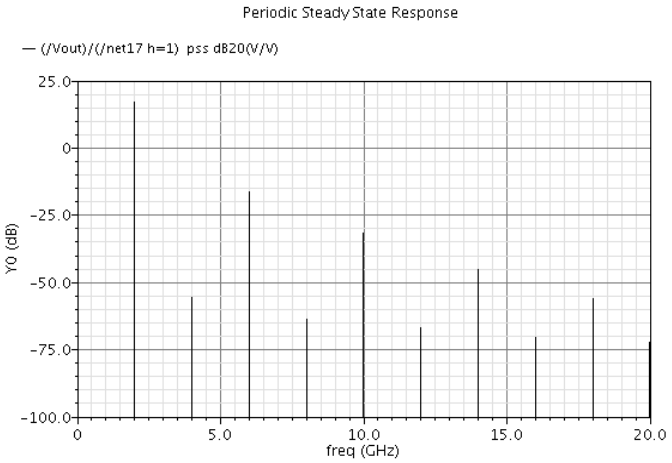


Fig. 4.1.1 Voltage gain at 1.8 V supply voltage

4.1.2 Power gain

It can be seen from the below graphs (Fig. 4.1.2) that the differential LNA has a power gain of approximately 21.42 dB at 1.8 V supply voltage, a center frequency of 2 GHz. To achieve required values for S_{11} and S_{22}, we have adjusted the sizes of inductors and capacitors. To meet required value of power gain to adjusted the sizes of transistor, inductors and capacitors. S11 and S22 shown in Fig 4.1.3 and Fig 4.1.4

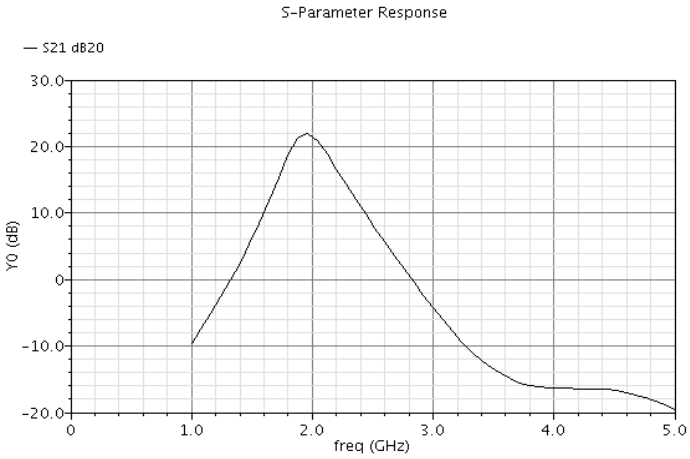


Fig. 4.1.2 Power gain at 1.8 V supply voltage

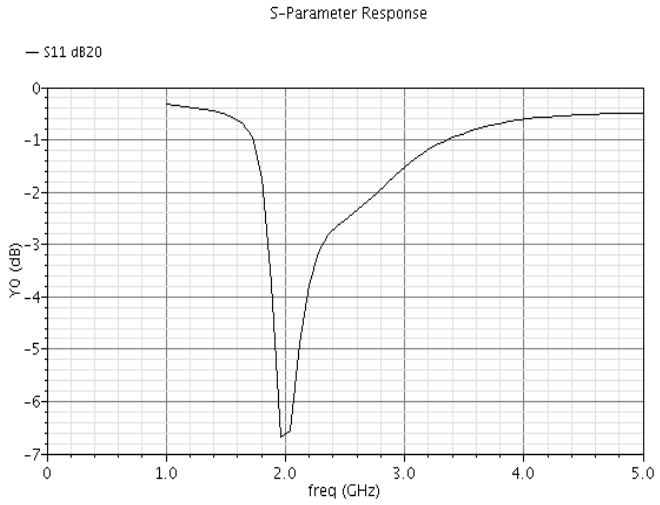


Fig. 4.1.3 S_{11} at 1.8 V supply voltage

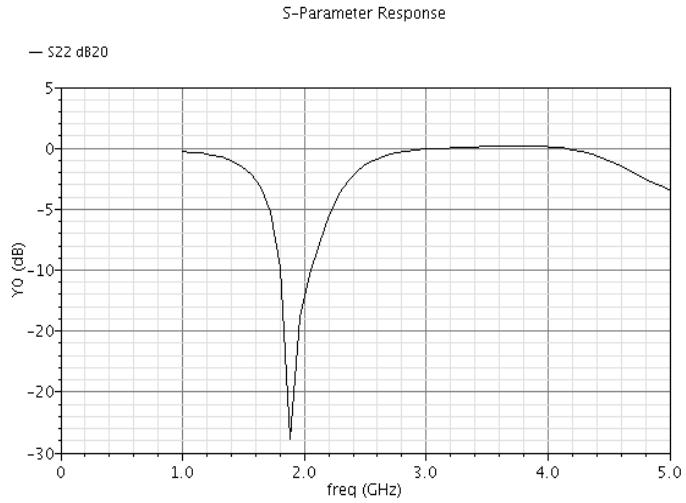


Fig. 4.1.4 S_{22} at 1.8 V supply voltage

4.4 Noise figure

S-parameter analysis was also used to generate the Noise Figure of the LNA. The minimum and actual noise figure of the LNA was simulated using scattering parameters. The graph below (Fig. 4.1.5 fig. 4.1.6) shows that the LNA has a noise figure (NF_{min}) and noise figure are of approximately 2.049 and 3.005 at 1.8 V supply voltage which is very close to its minimum noise figure at 2 GHz operating frequency. Since the LNA is adding minimal amount of noise the noise figure meets the specification.

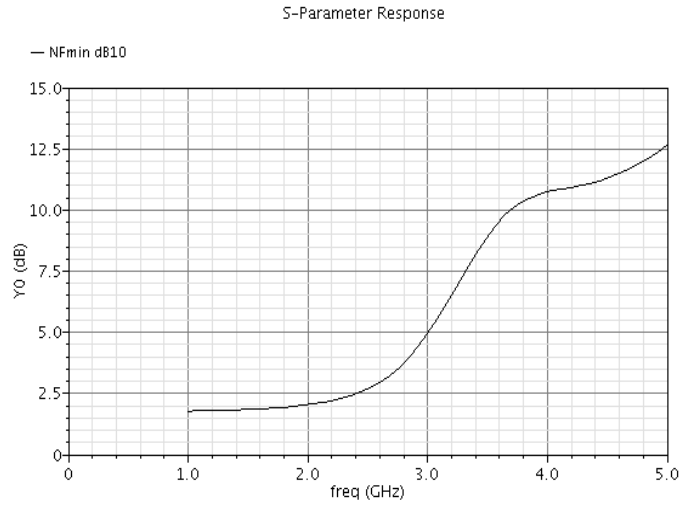


Fig. 4.1.5 Noise figure (NF_{min}) at 1.8 V supply voltage

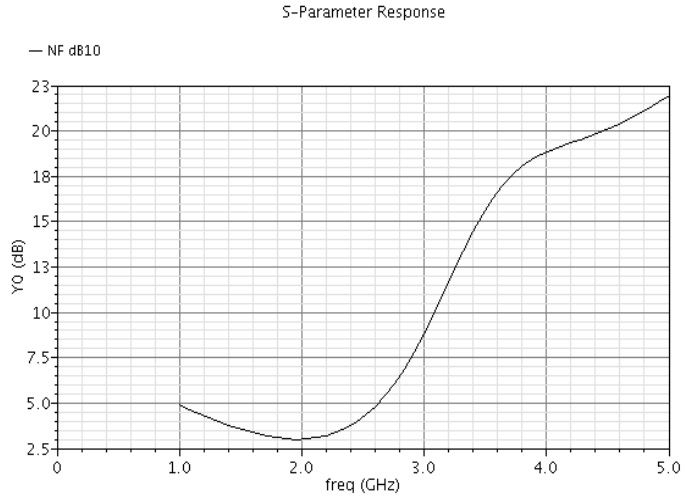


Fig. 4.1.6 Noise figure at 1.8 V supply voltage

4.5 Linearity

The linearity of the LNA was simulated using PSS analysis to find the 1 dB compression point and the third-order intercept point. The input power was swept from -40 dBm to 0 dBm. From the graph below (Fig. 1.4.7), the 1 dB compression point is the point at which the actual output power is 1 dB below the expected value for a linear amplifier. From the graph, the 1 dB compression point is -28.87 dBm at 1.8 V supply voltage. The third-order intercept point is the input power level at which the first and third order harmonics have the same output power level.

From the graph below (Fig. 4.1.8), the IIP3 point is -19.05 dBm at 1.8 v supply voltage, operating frequency is 2 GHz. To ensure that the amplifier is operating linearly, the circuit must have input power levels of around -30 dBm to 0 dBm. If the input power level reaches higher levels, the output signal will start to become distorted.

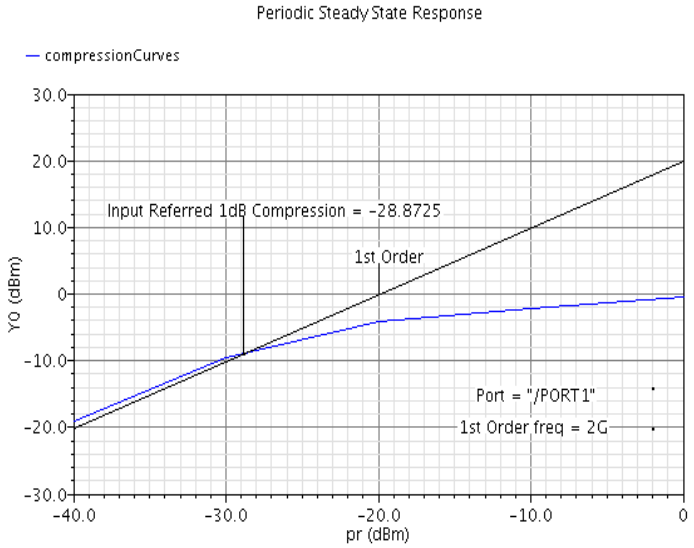


Fig. 4.1.7 1dB compression point at 1.8 V supply voltage

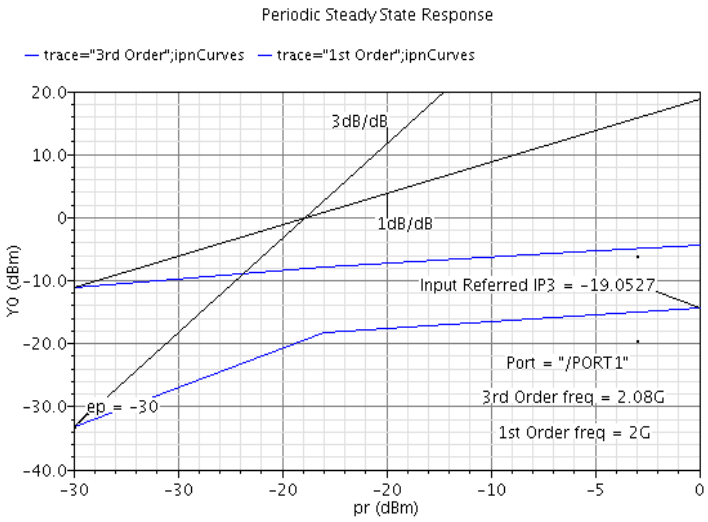


Fig. 4.1.8 IIP3 at 1.8 V supply voltage

4.2 Simulation wave forms of without inductively source degenerated differential LNA

The various simulation iterations are performed on the capacitor cross-coupled without source degenerated differential LNA circuit to meet design requirements. The simulation wave forms of capacitor cross-coupled without inductively source degenerated differential LNA operating at 2GHz frequency with supply voltage 1.8 V.

4.2.1 Voltage gain

The voltage gain was measured from the AC analysis as the difference in decibels between the output voltage and input voltage. It can be seen from the below graphs (Fig. 4.2.1) that the differential LNA has a voltage gain of approximately 13.615 dB at 1.8 V supply voltage, a center frequency of 2 GHz. This gain is sufficient to amplify any weak signal, but the gain will drop when layout is performed.

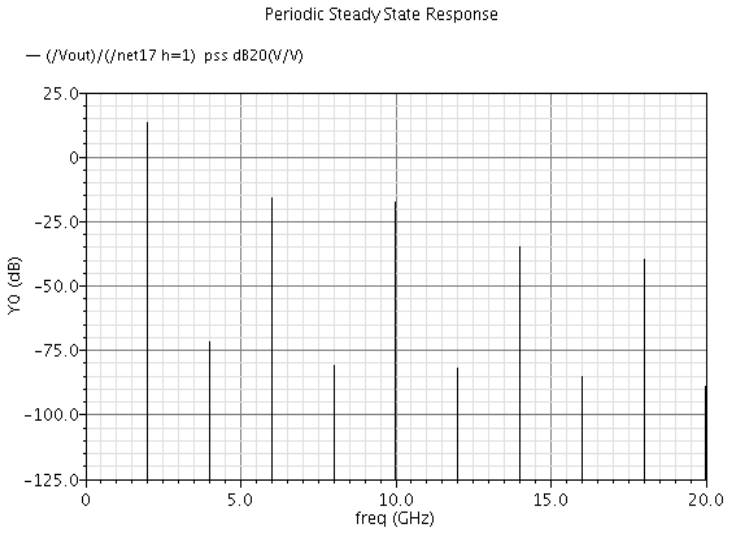


Fig. 4.2.1 Voltage gain at 1.8 V supply voltage

4.1.2 Power gain

It can be seen from the below graphs (Fig. 4.2.2) that the differential LNA has a power gain of approximately 23.28 dB at 1.8 V supply voltage, a center frequency of 2 GHz. To achieve

required values for S_{11} *and* S_{22}, we have adjusted the sizes of inductors and capacitors. To meet required value of power gain to adjusted the sizes of transistor, inductors and capacitors. The below graphs (Fig. 4.2.3 and Fig. 4.2.4 that the differential LNA of S_{11} and S_{22}.

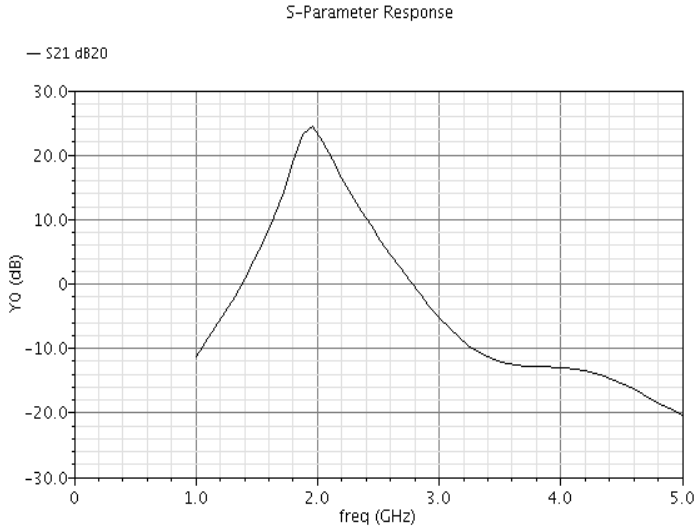


Fig. 4.2.2Power gain at 1.8 V supply voltage

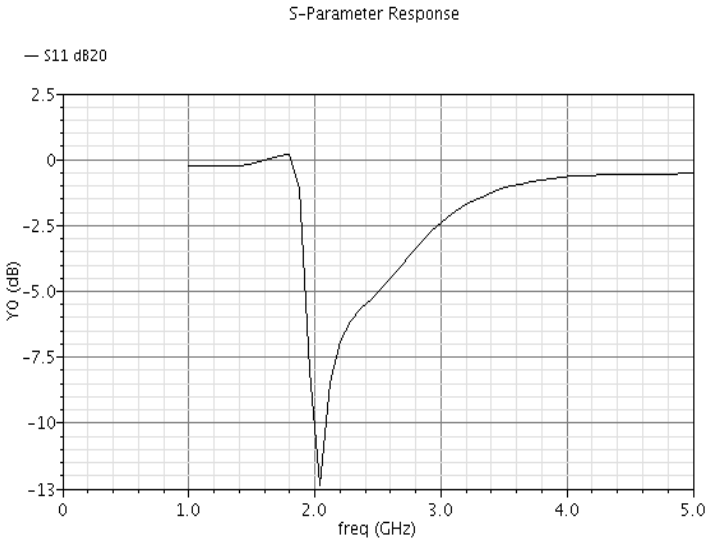


Fig. 4.2.3 S_{11} at 1.8 V supply voltage

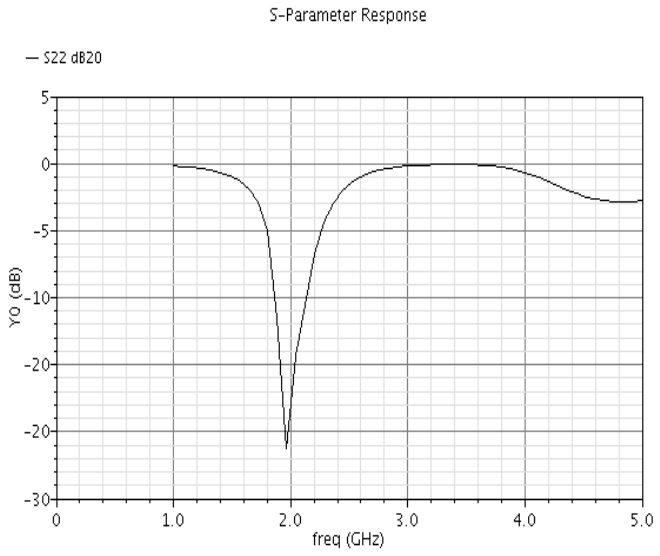


Fig. 4.2.4 S_{22} at 1.8 V supply voltage

4.4 Noise figure

S-parameter analysis was also used to generate the Noise Figure of the LNA. The minimum and actual noise figure of the LNA was simulated using scattering parameters. The graph below (Fig. 4.2.5 and Fig 4.2.6) shows that the LNA has a noise figure of approximately 1.984 at 1.8 V supply voltage which is very close to its minimum noise figure at 2 GHz operating frequency. Since the LNA is adding minimal amount of noise the noise figure meets the specification.

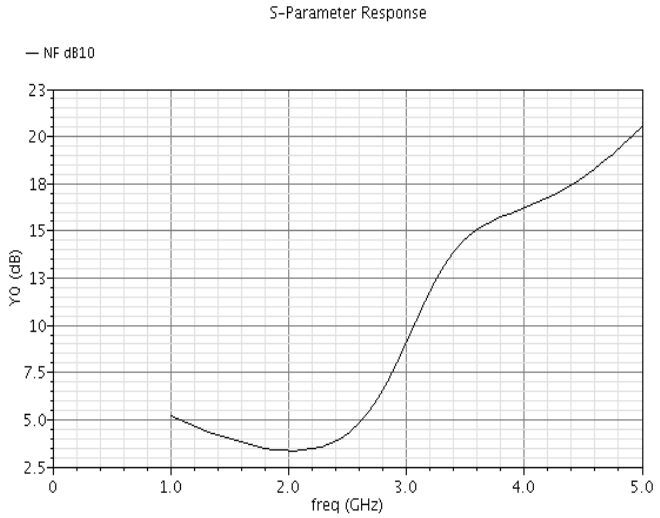


Fig. 4.2.5 Noise figure (NF_{min}) at 1.8 V supply voltage

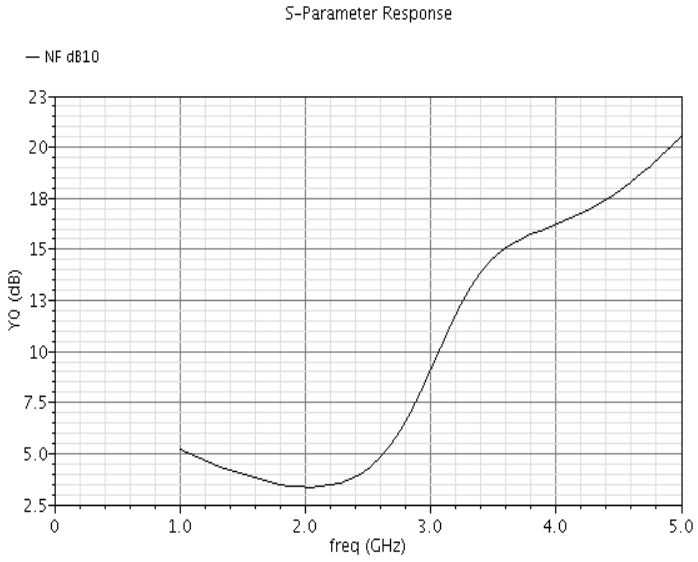


Fig. 4.2.6 Noise figure (NF_{min}) at 1.8 V supply voltage

4.5 Linearity

The linearity of the LNA was simulated using PSS analysis to find the 1 dB compression point and the third-order intercept point. The input power was swept from -40 dBm to 0 dBm. From the graph below (Fig. 4.2.7), the 1 dB compression point is the point at which the actual output power is 1 dB below the expected value for a linear amplifier. From the graph, the 1 dB compression point is -29.125 dBm at 1.8 V supply voltage. The third-order intercept point is the input power level at which the first and third order harmonics have the same output power level. From the graph below (Fig. 4.2.8), the IIP3 point is -18.5518 dBm at 1.8 v supply voltage, operating frequency is 2 GHz. To ensure that the amplifier is operating linearly, the circuit must have input power levels of around -30 dBm to 0 dBm. If the input power level reaches higher levels, the output signal will start to become distorted.

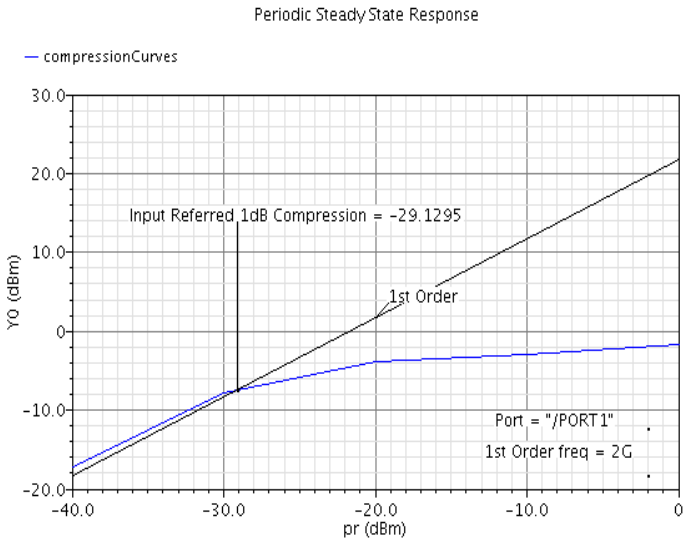


Fig. 4.2.7 1dB compression point at 1.8 V supply voltage

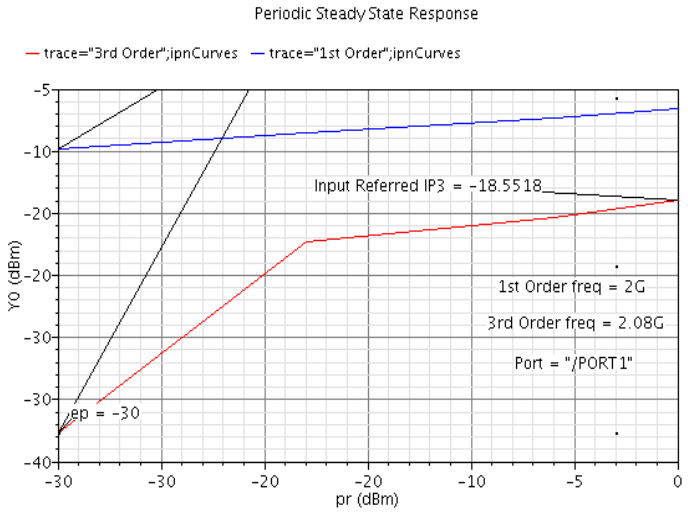


Fig. 4.2.8 IIP3 at 1.8 V supply voltage

4.6 Summary of Simulation Results

The various simulation iterations are performed on the capacitor cross-coupled differential cascode LNA circuit to meet design requirements. The simulation results of capacitor cross-coupled differential cascode LNA and the simulation results of post layout capacitor cross-coupled differential cascode LNA operating at 2GHz frequency and supply voltages are 1.5 V and 1.8 V. The performance results of simulations are compared to some other standard circuits reported. The proposed circuit is observed to consume low power in comparison to the existing circuits.

Parameters	Work done				[20]	[22]	[9]	[14]
	With inductively source degenerated		Without inductively source degenerated					
	Schematic	Post layout	Schematic	Post layout				
Noise Figure (NF_{min}) (dB)	2.049	6.138	1.984	5.623	1.47	2.0	2.4	1.87
Voltage gain (dB)	16.957	-2.485	13.615	-2.752	N.A	N.A	18.67	N.A
Power gain (dB)	21.42	1.972	23.28	2.31	12.63	18.9	15.87	10
S_{11} (dB)	-6.612	-38.97	-10.19	-4.83	-26.47	-10.62	-9.842	-13
Power consumption (mW)	6.055	4.145	5.852	4.161	6.49	6.45	16.2	16.2
IIP3 Point (dBm)	-19.05	-14.47	-18.55	-14.72	N.A	-13.2	-2.86	-2.05
Total input referred noise (V^2/Hz)	2.3046 e^{-18}	3.5428 e^{-18}	3.0305 e^{-18}	3.6571 e^{-18}	N.A	N.A	5.0539 e^{-19}	N.A
Frequency (GHz)	2	2	2	2	2.4	2.47	2	2.2
CMOS Process (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.35
Supply voltage (V)	1.8	1.8	1.8	1.8	1.2	1.5	1.8	1.8

Table 3: Simulation Results

CHAPTER 5

Layout

With the LNA designed, the final step was the layout process. The layout process allows designers to have their circuits manufactured. Layout is an important step in RFIC design for several reasons. Layout determines the physical area that the LNA will occupy which is important as there are chip size specifications for LAN. More importantly, the physical layout of the LNA will have a direct impact on its performance. The performance is affected as the physical layout introduces parasitics, coupling, matching as an issue and many other factors noted included in the design of the LNA [23].

5.1 Layout Background

Layout was performed using the Cadence layout tool. The process that was used, allows for 6 levels of metal to be used; the first level of metal is the most resistive while the top level of metal, the analog metal, is the least resistive. The metals are separated by a polysilicon layer. A connection between the metal layers is achieved using via. Via provide a path from one metal to another, however they introduce resistance. To minimize the resistance, an array of via can be implemented [23].

The RF inductors used in the design of the LNA were built using the analog metal, while the RF Metal-Insulator-Metal (MIM) capacitors were built using two metal layers separated by polysilicon. The layout of the transistors was performed by Cadence with connections to the base, emitter and collector through the first and second levels of metal. The resistors used in the LNA design were built in layout using polysilicon with connections at its terminals through metal 1.

The signal paths made of the metals can be characterized as resistors. Like any metal, the resistance is higher the thinner and longer the metal is while the resistance is lower when the metal is wider and shorter. It is advantageous to have the RF signals or signals traveling a long distance on the chip transmitted between components in the analog metal. This would ensure that any losses would be minimized. Conversely, DC paths can be implemented using the lower level, more resistive metals [23]. Electrons flow with greater ease in straight paths; therefore, to

minimize losses in the RF signal their paths should be as straight as possible. As well, electron movement can cause the path's atoms to move, known as electro migration. Over time if enough metal is moved there can be a loss of contact between metal paths [24]. Therefore, each metal level has a required width per mA of DC current flowing in the path.

5.2 Layout Process

The first step in the process was to generate a layout which transformed all of the components from the schematic into their physical layout. Since the LNA is differential, the two sides of the amplifier must be mirrored to ensure that they are matched in terms of where components are placed, the size and placement of their paths, etc. as best as possible. If the two sides are not identical, parasitics in the differential pair will not be equal and the amplification of the input signals potentially could be unequal.

Once the layout was generated, the components were moved into positions that would be advantageous. To ensure that the RF signal has a straight path, the components which have RF signals flowing through them were placed in the middle of the layout with the input signals being fed at the bottom of the circuit and the output pins were placed at the top of the RF path, as shown in Fig 5.2.1 and Fig 5.2.2. As well, the RF components were placed so that the RF signals would have to travel the shortest possible distance.

Multiple pins ensure that the path lengths from the pins to the components were minimized. Finally, each pin had a bond pad connected, allowing the circuit to have connections off chip after fabrication. The completed layout is shown in Fig 5.2.1 and 5.2.2. The next step in layout was connecting all of the nets from the schematic. With the help of Cadence, all of the incomplete nets between components were identified. Metal paths were used to connect the components. To minimize losses, RF signals were transmitted in the analog metal and in straight paths, as much as possible. Arrays of via between the metal layers were used as much as possible since a single via has a higher resistance than an array of via.

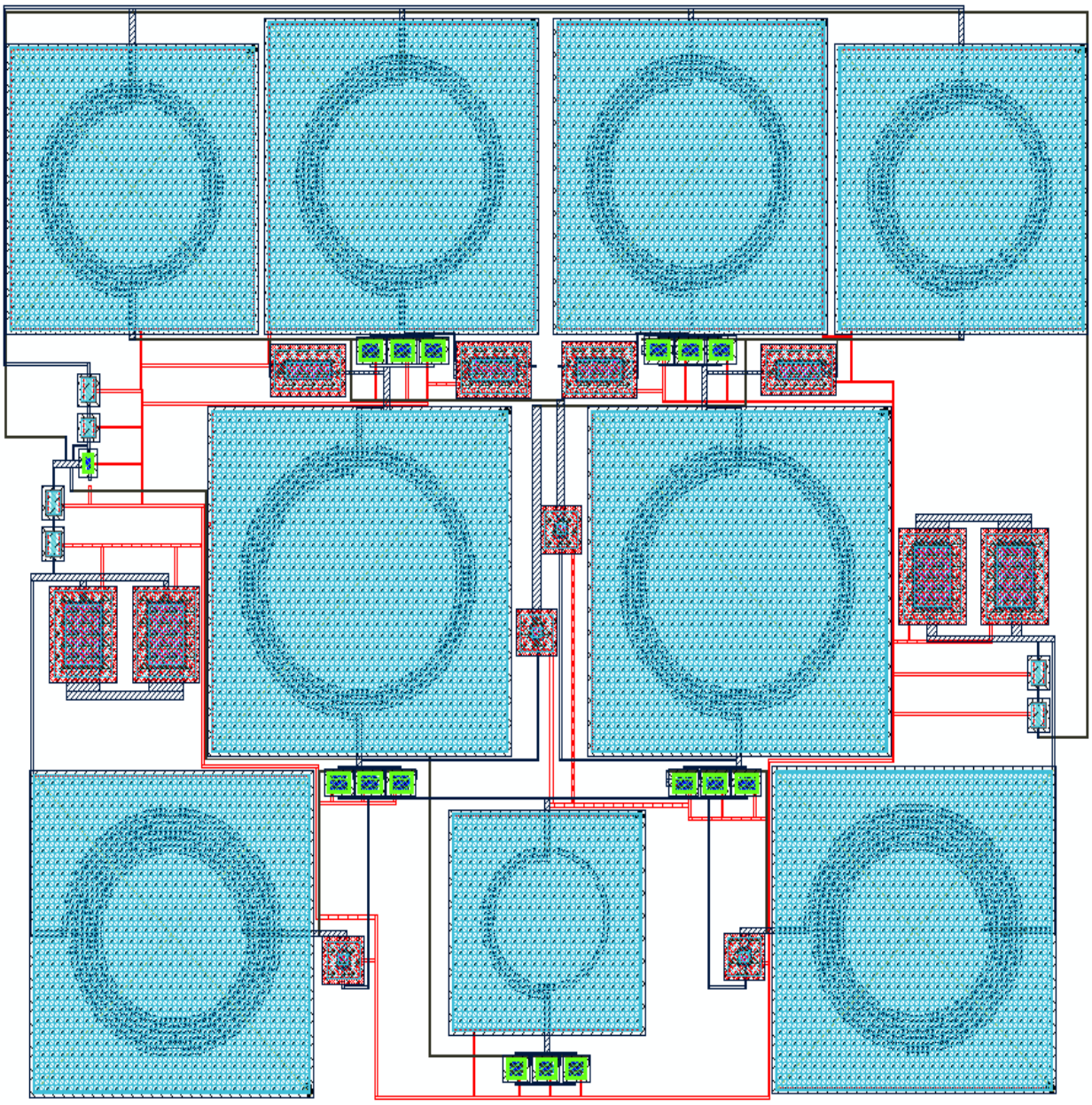


Fig. 5.2.1. Layout of capacitor cross-coupled with inductively source degenerated differential cascade LNA

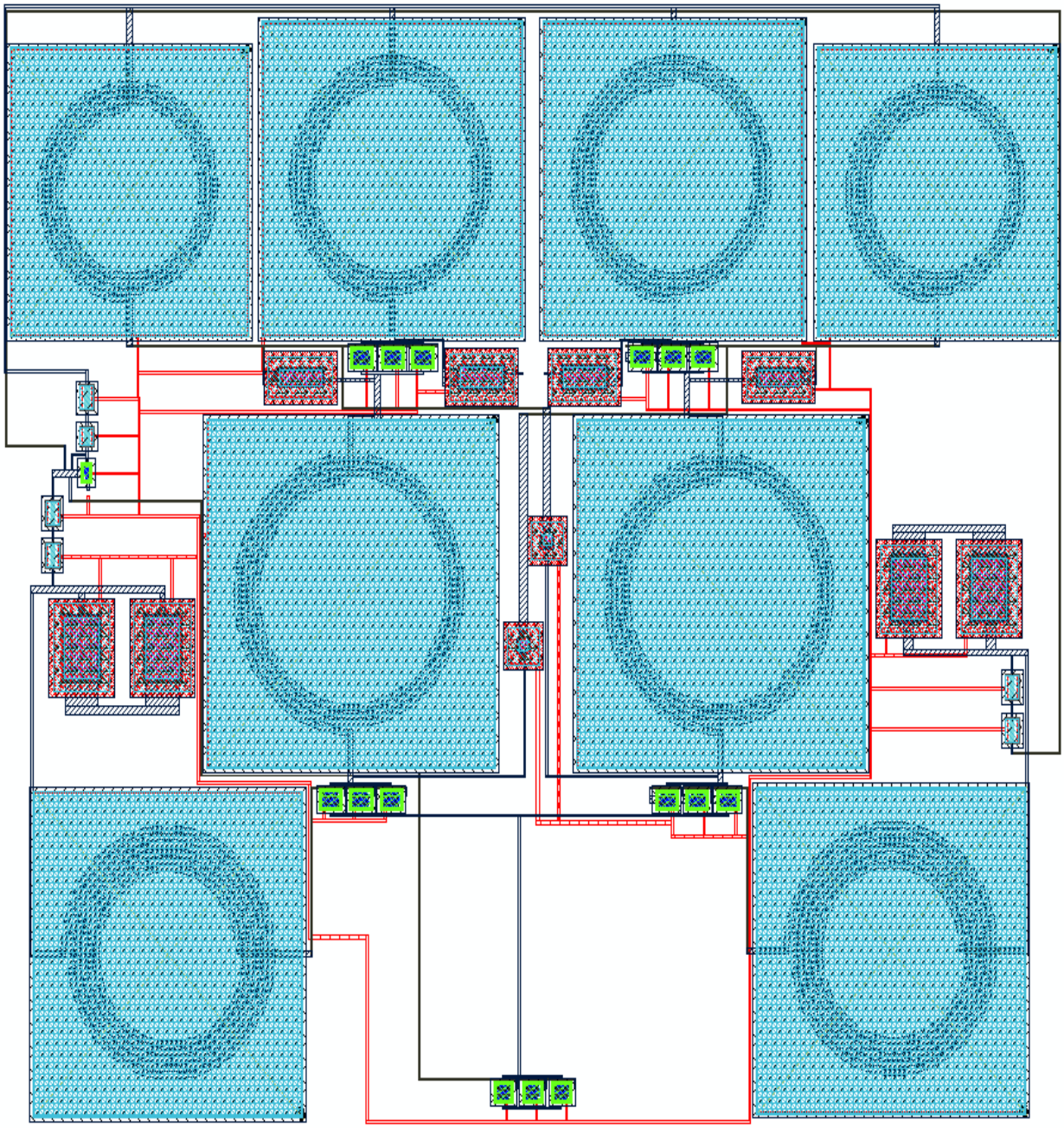


Fig. 5.2.2. Layout of capacitor cross-coupled without inductively source degenerated differential cascade LNA

5.3 Design Rule Check (DRC)

Once the layout was generated and the incomplete nets were connected, the next step was to verify that the layout met the design rules of the fabrication process. The design rules specify the limitations of fabrication using the particular process. This verification was performed using the DRC function of Cadence. The DRC test compares the layout to the design rules of the process. When first performed, there were hundreds of DRC errors. Through iterations, these errors were reduced. However, several errors concerning the bond pads were created. At this point, the layout process was complete.

CONCLUSION

In this work, a capacitor cross-coupled with inductively source degenerated differential cascode LNA and capacitor cross-coupled without inductively source degenerated differential cascode LNA has been presented. The simulations of the circuit are carried out using UMC 0.18 µm CMOS process. The differential LNA design, we obtained a noise figure, power consumption, voltage gain and power gain at different supply voltages 1.5 V and 1.8 V are reported here. In this design the gain depends on source inductance and Inter-stage inductor between input stage and cascoded stage boost gain and lower noise figure. The performance results of simulations are reported. The proposed circuit is observed to consume low power in comparison to the existing circuits.

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